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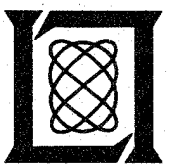

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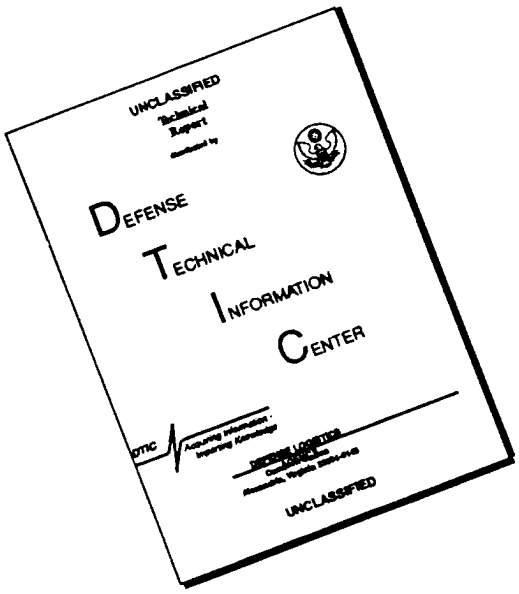

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The ESC Public Affairs Office has reviewed this report, and it is releasable to the National Technical Information Service, where it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

Gary Tutungian
Administrative Contracting Officer
Contracted Support Management

ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 May through 31 July 1995. The topics covered are Electrooptical Devices, Quantum Electronics, Materials Research, Submicrometer Technology, High Speed Electronics, Microelectronics, Analog Device Technology, and Digital Integrated Circuits. Funding is provided primarily by the Air Force, with additional support provided by the Army, ARPA, Navy, BMDO, NASA, and NIST.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

SOLID STATE RESEARCH

QUARTERLY TECHNICAL REPORT

1 MAY–31 JULY 1995

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INTRODUCTION

1. ELECTROOPTICAL DEVICES

A mass-transported microlens array fabricated on a planar substrate has been attached directly to a laser heatsink. This novel packaging approach has produced a compact laser assembly for collimated laser output.

2. QUANTUM ELECTRONICS

A compact, low-threshold, multipass optical parametric amplifier has been developed for the conversion of short-pulse 1064-nm Nd:YAG laser radiation into eyesafe 1572-nm radiation for laser ranging and radar applications. The amplifier has a threshold pump power of 45 μJ, and at 3 to 4 times this threshold pump power it converts 30% of the input 1064-nm radiation into output 1572-nm radiation.

3. MATERIALS RESEARCH

A photoelectrochemical technique has been developed for maskless etching of almost arbitrary profiles into the surface of Si wafers. The fabrication of microlens arrays has been demonstrated by the new technique, which may offer important advantages over mask-based methods in fabrication of optical elements, sensors, and other micromechanical structures.

High-quality, mirror-smooth AlGaAs epilayers with strong room-temperature photoluminescence have been grown at 650°C by low-pressure organometallic vapor phase epitaxy with a new aluminum precursor tritertiarybutylaluminum. Nominally undoped AlGaAs layers have exhibited *n*-type conductivity with electron concentrations at ~ $1–5 \times 10^{16}$ cm^{-3}, with no detectable carbon and low ($< 3 \times 10^{17}$ cm^{-3}) oxygen concentrations, which make TTBAl very attractive for low-temperature growth of Al-containing III-V alloys.

4. SUBMICROMETER TECHNOLOGY

Sub-0.25-μm polysilicon features have been patterned at 193 nm using silylated resist as an etch mask. The dry etch process has been optimized resulting in vertical and notchless profiles with 500:1 polysilicon:oxide selectivity.

Nanocrystalline silicon aggregates embedded in a predominantly amorphous silicon layer have been observed in anodically etched *p*-Si(100) by using valence band x-ray photoelectron spectroscopy and lattice-imaged high-resolution transmission electron microscopy. A crystalline-to-amorphous phase transition, accompanied by a significant decrease in photoluminescent yield, occurs after exposure to x-radiation.

5. HIGH SPEED ELECTRONICS

Field-emitter arrays (FEAs) incorporating a number of processing improvements have been fabricated with high yields and have provided emission currents as high as 2 mA. The FEAs are being developed for use as cathodes in a klystrode microwave tube.

6. MICROELECTRONICS

Measurements of the quantum efficiency and optical response uniformity of a back-illuminated wafer-scale charge-coupled device imager have been performed. The quantum efficiency peaks at about 90% at 600 nm and is 65% for an average that is weighted with the solar photon flux over the range 300–1000 nm, and the optical response nonuniformity is less than 1.5% rms for solar illumination.

7. ANALOG DEVICE TECHNOLOGY

The dispersive delay of a 2-GHz-bandwidth high-temperature superconductive (HTS) chirp filter has been increased to 40 ns using an improved wafer bonding and thinning technique to physically support the 125-μm-thick, 2-in.-diam $LaAlO_3$ substrates that form the filter's stripline structure. This HTS chirp filter, with a time-bandwidth product of 80, has enabled consideration of a compressive-cryoreceiver concept for electronic warfare and electronic intelligence applications.

8. DIGITAL INTEGRATED CIRCUITS

A sub-0.5-μm CMOS process has been developed for research in fast, low-power, mixed analog/digital circuit design. An 800-MHz CMOS amplifier and 0.3-μm transistors have been demonstrated, and fabrication has begun on circuits designed at five different institutions.

REPORTS ON SOLID STATE RESEARCH

1 MAY THROUGH 31 JULY 1995

PUBLICATIONS

Suppressed Gate Current in a Superlattice-Insulated-Gate Field-Effect Transistor on InP	E. R. Brown C. L. Chen L. J. Mahoney P. A. Maki K. B. Nichols	*Appl. Phys. Lett.* **66**, 2352 (1995)
InAsSb/InAlAs Strained Quantum-Well Lasers Emitting at 4.5 μm	H. K. Choi G. W. Turner H. Q. Le	*Appl. Phys. Lett.* **66**, 3543 (1995)
The Three-Terminal Fuse: A New Switching Device	S. S. Cohen	*IEEE Trans. Electron Devices* **42**, 1352 (1995)
YBCO/Ferrite Low-Loss Microwave Phase Shifter	G. F. Dionne D. E. Oates D. H. Temme	*IEEE Trans. Appl. Superconduct.* **5**, 2083 (1995)
Electron Field Emission from Diamond and Other Carbon Materials after H_2, O_2, and Cs Treatment	M. W. Geis J. C. Twichell J. Macaulay* K. Okano*	*Appl. Phys. Lett.* **67**, 1328 (1995)
Basic Module for an Integrated Optical Phase Difference Measurement and Correction System	B. Golubovic* J. P. Donnelly C. A. Wang W. D. Goodhue R. H. Rediker*	*IEEE Photon. Technol. Lett.* **7**, 649 (1995)
193-nm Lithography at MIT Lincoln Lab	M. Hibbs* R. R. Kunz M. Rothschild	*Solid State Technol.* **38** (7), 69 (1995)

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High-Power High-Temperature Superconducting Microstrip Filters for Cellular Base-Station Applications	G.-C. Liang* D. Zhang* C.-F. Shih* M. E. Johansson* R. S. Withers* A. C. Anderson D. E. Oates	*IEEE Trans. Appl. Superconduct.* **5**, 2652 (1995)
Mass-Transport Fabrication of Large-Numerical-Aperture Microoptics	Z. L. Liau	*Proc. SPIE* **2383**, 310 (1995)
Microwave Subsystems Developed Through the Consortium for Superconducting Electronics	R. W. Ralston	*Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductivity,* Vol. 95-9 (Electrochemical Society, Pennington, N.J., 1995), p. 3
Superconducting Cueing Receiver for Space Experiment	T. C. L. G. Sollner W. G. Lyons D. R. Arsenault A. C. Anderson M. M. Seaver R. R. Boisvert R. L. Slattery	*IEEE Trans. Appl. Superconduct.* **5**, 2071 (1995)
A Josephson-Junction-Bridge Track-and-Hold Circuit	K. Y. Tam J. P. Sage	*IEEE Trans. Appl. Superconduct.* **5**, 3172 (1995)
High-Density 300-Gbps/cm^2 Parallel Free-Space Optical Interconnection Design Considerations	D. Z. Tsang	*Optical Computing, 1995 OSA Technical Digest Series,* Vol. 10 (Optical Society of America, Washington D.C., 1995), p. 277

*Author not at Lincoln Laboratory.

Uniform Linear Arrays of Strained-Layer InGaAs–AlGaAs Quantum-Well Ridge-Waveguide Diode Lasers Fabricated by ECR-IBAE	J. D. Woodhouse C. A. Wang J. P. Donnelly D. Z. Tsang R. J. Bailey D. E. Mull K. Rauschenbach O. A. Popov*	*IEEE J. Quantum Electron.* **31**, 1357 (1995)

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Microwave Applications of Photonic Crystals	E. R. Brown O. B. McMahon C. D. Parker C. D. Dill III	In *Photonic Band-Gap Materials*, C. Soukoulis, ed. (Kluwer Academic, Dordrecht, Netherlands)
Tunable Single-Frequency Yb:YAG Laser with 1-W Output Power Using Twisted Mode Technique	T. Y. Fan J. Ochoa	*IEEE Photon. Technol. Lett.*
Spectral Linewidth of a Free-Running CW Single-Frequency External-Cavity Quantum Well InGaAs/AlGaAs Diode Laser	L. Hsu* A. Mooradian R. L. Aggarwal	*Opt. Lett.*
Fabrication of Two-Sided Anamorphic Microlenses and Direct Coupling of Tapered High-Power Diode Laser to Single-Mode Fiber	Z. L. Liau J. N. Walpole J. C. Livas E. S. Kintzer	*IEEE Photon. Technol. Lett.*
Ho:YAG Laser Pumped by 1.9-μm Diode Lasers	C. D. Nabors* T. Y. Fan A. Sanchez H. K. Choi G. W. Turner	*IEEE J. Quantum Electron.*

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193-nm Lithography	M. Rothschild A. R. Forte M. W. Horn R. R. Kunz S. C. Palmateer J. H. C. Sedlacek	*IEEE J. Quantum Electron.*
Tritertiarybutylaluminum as an Organometallic Source for Epitaxial Growth of AlGaSb	C. A. Wang M. C. Finn S. Salim* K. F. Jensen* A. C. Jones*	*Appl. Phys. Lett.*

PRESENTATIONS†

Diamond Cold Cathodes: Experiment and Theory	M. W. Geis J. C. Twichell N. N. Efremow K. E. Krohn C. A. Marchi T. M. Lyszczarz	High Definition Information Exchange Conference, Arlington, Virginia, 30 April–3 May 1995
Fabrication of Large-Area CCD Detectors on High-Purity, Float-Zone Silicon	J. A. Gregory B. E. Burke M. J. Cooper R. W. Mountain B. B. Kosicki	7th European Semiconductor Detector Conference, Schloss Elamau, Germany, 7-10 May 1995
Electrical Properties of the Hydrogen Defect in InP and the Microscopic Structure of the 2316 cm^{-1} Hydrogen Related Line	D. F. Bliss* G. G. Bryant* D. Gabbe* G. W. Iseler E. E. Haller* F. X. Zach*	7th International Conference on InP and Related Materials, Sapporo, Japan, 9-13 May 1995
Fabrication of Large-Area CCD Detectors on High-Purity, Float-Zone Silicon	J. A. Gregory B. E. Burke M. J. Cooper R. W. Mountain B. B. Kosicki	European Southern Observatory Detector Conference, Garching, Germany, 11 May 1995

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†Titles of presentations are listed for information only. No copies are available for distribution.

Wideband Compressive Receiver Based on Advanced Superconductor and Semiconductor Circuits	W. G. Lyons D. R. Arsenault T. C. L. G. Sollner R. W. Ralston	1995 IEEE MTT-S International Microwave Symposium, Orlando, Florida, 15-19 May 1995
Systems Implications of SCT Frequency Agile Superconducting Thin Film (FAST™) Filter Technology	R. M. Yandrofski* G. A. Koepf* D. O. Patton* R. R. Bonetti* W. G. Lyons	
Optical Analog Links Using Linearized Modulators for Antenna Remoting	G. E. Betts F. J. O'Donnell K. G. Ray	IEEE Antennas and Propagation Society Symposium, Newport Beach, California, 18-23 June 1995
Ytterbium Lasers	T. Y. Fan	Lincoln Laboratory Technical Seminar Series, City University of New York, 19 May 1995
Coherent Terahertz Generation Using Low-Temperature-Grown GaAs Photomixers	E. R. Brown K. A. McIntosh K. B. Nichols O. B. McMahon W. F. DiNatale T. M. Lyszczarz A. Pine* R. Suenram*	1995 Conference on Lasers and Electro-Optics, Baltimore, Maryland, 21-26 May 1995
InAsSb Strained Quantum-Well Lasers Emitting in the 4-μm Band	H. K. Choi G. W. Turner H. Q. Le	
Analysis of Multiple-Input N × M Waveguide Couplers with Multimode Guiding Sections	E. R. Thoen* L. A. Molter* J. P. Donnelly	

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Electro-Optically Q-Switched Nd:YVO_4 Microchip Lasers	J. J. Zayhowski C. Dill III	1995 Conference on Lasers and Electro-Optics, Baltimore, Maryland, 21-26 May 1995
UV Generation with Passively Q-Switched Picosecond Microchip Lasers	J. J. Zayhowski J. Ochoa C. Dill III	
High-Power (1.3-W) Optically Pumped Midwave-Infrared (3.4-μm) $InAs/InAs_xSb_{1-x}$ Superlattice Lasers	Y.-H. Zhang* H. Q. Le	
Broad-Band Four-Wave Mixing in Semiconductor Waveguides	H. Q. Le	1995 Quantum Electronics and Laser Science Conference, Baltimore, Maryland, 21-26 May 1995
Profile Control of High Aspect Ratio Resist Structures	M. B. Stern S. C. Palmateer M. W. Horn M. Rothschild B. E. Maxwell J. E. Curtin	39th International Symposium on Electron, Ion and Photon Beams, Scottsdale, Arizona, 30 May–3 June 1995
Diamond Field-Emission Cathodes	M. W. Geis J. C. Twichell M. B. Stern N. N. Efremow K. E. Krohn T. M. Lyszczarz R. Uttaro	12th North Coast Symposium, NASA, Cleveland, Ohio, 1 June 1995
Device Application Issues for High-T_c Passive Microwave Circuits	W. G. Lyons	Canadian Institute for Advanced Research Summer School, Hamilton, Ontario, Canada, 1-2 June 1995
YBCO/Ferrite Low-Loss Microwave Phase Shifter	W. G. Lyons	

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High-Density Gated Field-Emitter Arrays	C. O. Bozler D. D. Rathman C. T. Harris G. A. Lincoln S. Rabe R. A. Murphy M. A. Hollis	IEEE International Conference on Plasma Science, Madison, Wisconsin, 5-8 June 1995
Diamond Field-Emission Cathodes	M. W. Geis J. C. Twichell M. B. Stern N. N. Efremow K. E. Krohn T. M. Lyszczarz R. Uttaro	American Vacuum Society Annual Symposium, Boston, Massachusetts, 12-13 June 1995
The Role of MIT Lincoln Laboratory's Microelectronics Laboratory in Supporting Today's Semiconductor Process Research and Development	C. L. Keast	Meeting of the New England Chapter, American Vacuum Society, Burlington, Massachusetts, 13 June 1995
Diamond Cold Cathodes: Experiment and Theory	M. W. Geis J. C. Twichell N. N. Efremow K. E. Krohn C. A. Marchi T. M. Lyszczarz	Technical Seminar, Texas Instruments, Dallas, Texas, 18 June 1995
Tritertiarybutylaluminum as a New Organometallic Source for Epitaxial Growth of AlGaSb	C. A. Wang M. C. Finn S. Salim* K. F. Jensen* A. C. Jones*	37th Electronic Materials Conference, Charlottesville, Virginia, 21-23 June 1995
Quasi-Three-Level Lasers	T. Y. Fan	New Perspectives in Laser Sources and Applications, St. Andrews, Scotland, 25 June–7 July 1995
Tutorial on Diode-Pumped Solid-State Lasers	T. Y. Fan	

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Solid-State Laser Technology Development at Lincoln Laboratory	T. Y. Fan J. J. Zayhowski A. Sanchez	1995 Coherent Laser Radar Conference, Keystone, Colorado, 23-27 July 1995
Gated Field-Emitter Arrays for Microwave-Tube Applications	C. O. Bozler D. D. Rathman C. T. Harris G. A. Lincoln R. H. Mathews S. Rabe R. A. Murphy M. A. Hollis H. I. Smith*	8th International Vacuum Microelectronics Conference, Portland, Oregon, 30 July–3 August 1995
Diamond Field-Emission Cathodes	M. W. Geis J. C. Twichell M. B. Stern N. N. Efremow K. E. Krohn T. M. Lyszczarz R. Uttaro	

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1. ELECTROOPTICAL DEVICES

1.1 COMPACT DIODE LASER ASSEMBLY WITH CONTACT MICROLENS FOR COLLIMATED LIGHT OUTPUT

The advancement of semiconductor laser materials growth and device fabrication technology has brought the cost of the laser chip well below the cost of the associated optics, precision alignment, and packaging required to effectively utilize the device in systems applications. We report here initial results on a novel compact diode laser packaging approach that utilizes unique microlenses to simplify the lens alignment and packaging. In this scheme, a microlens fabricated on a planar substrate is directly attached to the laser heatsink to form a precision optical assembly providing a collimated or focused output beam. The approach is applicable to either single lasers or laser arrays.

Microlenses are typically used to collimate or focus the output of semiconductor diode lasers. For maximum efficiency the lens must be precisely aligned with regard to *xyz* translation and to tip and tilt angle. In our approach, shown in Figure 1-1, a mass-transport lenslet fabricated on a planar substrate is mounted on the device to automatically reduce the number of alignment operations. For a collimated laser output the lenslet is designed to have a focal length *f* equal to the substrate thickness. The lens is placed in direct contact with the laser chip and its heatsink, thereby eliminating the need for a separate lens mounting fixture. The laser can be mounted either flush with the edge or allowed to extend several micrometers beyond the heatsink, as shown. If the chip protrudes a few micrometers beyond the heatsink, the lens will pivot on the lower edge of the laser chip and contact the heatsink only along its lower edge.

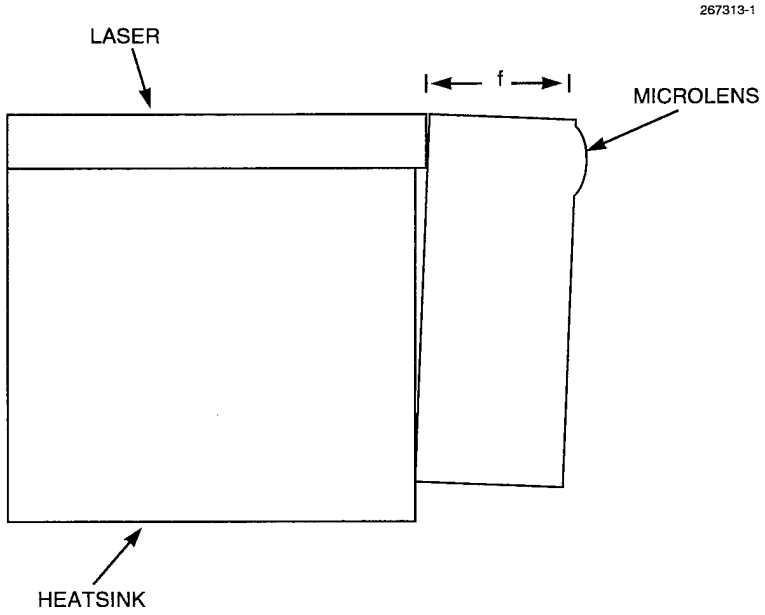

Figure 1-1. Diagram showing diode laser and lens assembly with direct contact between laser and lens. In this approach a microlens fabricated on a planar substrate is attached to the laser heatsink.

To minimize the effect of misalignment caused by variations in the position of the laser that change the object distance and tilt the lens, the distance from the pivot point to the contact point should be much larger than the protrusion of the laser and, for lasers mounted stripe up, the thickness of the laser chip.

Mass-transported GaP microlenses [1],[2] are very attractive for this application because they can be made with high numerical aperture (NA) for good light collection efficiency and because the high refractive index of GaP allows much looser tolerances on the crucial thickness of the lens compared to lower-index materials. For the 0.46-NA lens used in this experiment, the thickness should be within about $\pm$ 4 μm. The microlenses were fabricated in two-dimensional arrays with a nominal diameter of 140 μm on a pitch of 300 μm. The lens wafer was very carefully polished to a thickness of 423 μm. The lens array chip was 2 mm long in the vertical direction to minimize tilt misalignment. The lenses were coated for low reflection with a quarter-wavelength thickness of SiO_2.

For this initial demonstration we used an edge-emitting 980-nm ridge-waveguide laser array with a pitch of 150 μm. The array was soldered to a heatsink using conventional die attachment techniques with attention to ensure that the solder did not flow beyond the laser output facet and interfere with subsequent lens attachment. In this case, each edge of the laser array protruded 10 mm above the heatsink and the 68-μm-thick laser chip was mounted stripe up. The lens array was actively aligned to the laser array with micropositioners. The lateral and transverse positions and the rotation of the lens array were adjusted such that each lens was centered on a laser emitter. No adjustment of the lens position along the z-axis in the direction of laser emission or of the tip and tilt angle of the lens was necessary because those are set by the fabrication of the lens and the mounting arrangement. The lens was attached directly to the laser heatsink with ultraviolet-curable adhesive. The heatsink is Au-coated silicon with a lapped and polished flat edge used for the lens attachment surface. The tilt of the lens relative to the heatsink can be estimated from the laser protrusion and the length of the lens array chip to be about 0.3°. In the composite infrared and visible photograph of the assembly in Figure 1-2, two of the lasers are covered by a lens and are collimated, while the other two are not aligned to a lens. In Figure 1-3, far-field scans taken in the directions parallel and perpendicular to the laser junction have a full width at half-maximum of about 0.8° and 0.6°, respectively, much narrower than the far-field pattern of the laser without the lens. The far-field pattern is narrower perpendicular to the junction because the lens is more completely filled by the wider divergence of the laser in that direction.

Estimates of the effects of misalignment based on optical path length differences for this approach are encouraging. Lens aberrations and misalignments can produce optical path length differences that result in phase front distortions that are large enough to reduce coupling efficiencies to single-mode fiber. While biconvex lenses can be corrected for spherical aberration with the lens centered on the laser, significant phase front distortions can still result if the lens is laterally misaligned even slightly, e.g., 1 μm off axis. By using this approach with planoconvex lenses, the high refractive index of the GaP allows light rays to remain paraxial even at relatively large numerical aperture, and the phase front distortion can remain small. For the lens used in this experiment, the maximum distortion at the edge of the lens is estimated to be no more than $\lambda/10$ over lateral misalignments of $\pm$ 10 μm. Negligible phase front distortions are important for applications such as efficient coupling to single-mode fiber.

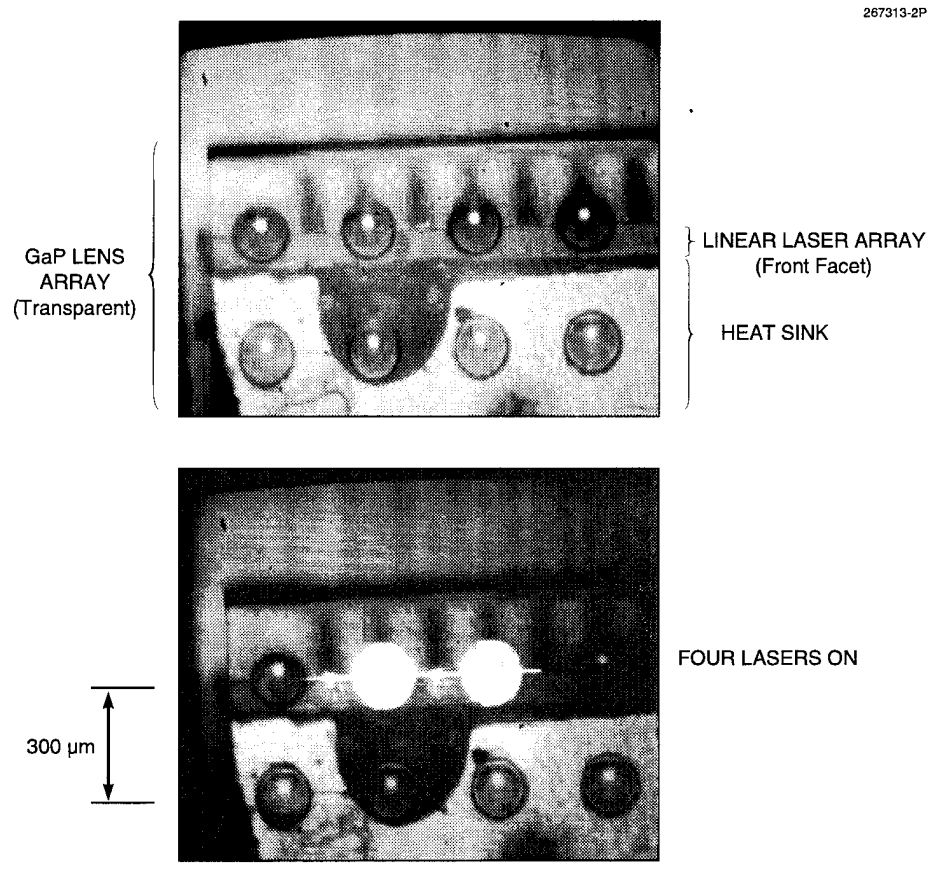

Figure 1-2. Photographs of assembly in which the GaP lens array contacts the laser array. Although covered by the lens, the laser array is visible because the GaP is transparent. The lasers have twice the pitch of the lenses so that only two of the four lasers are collimated by the lenslets.

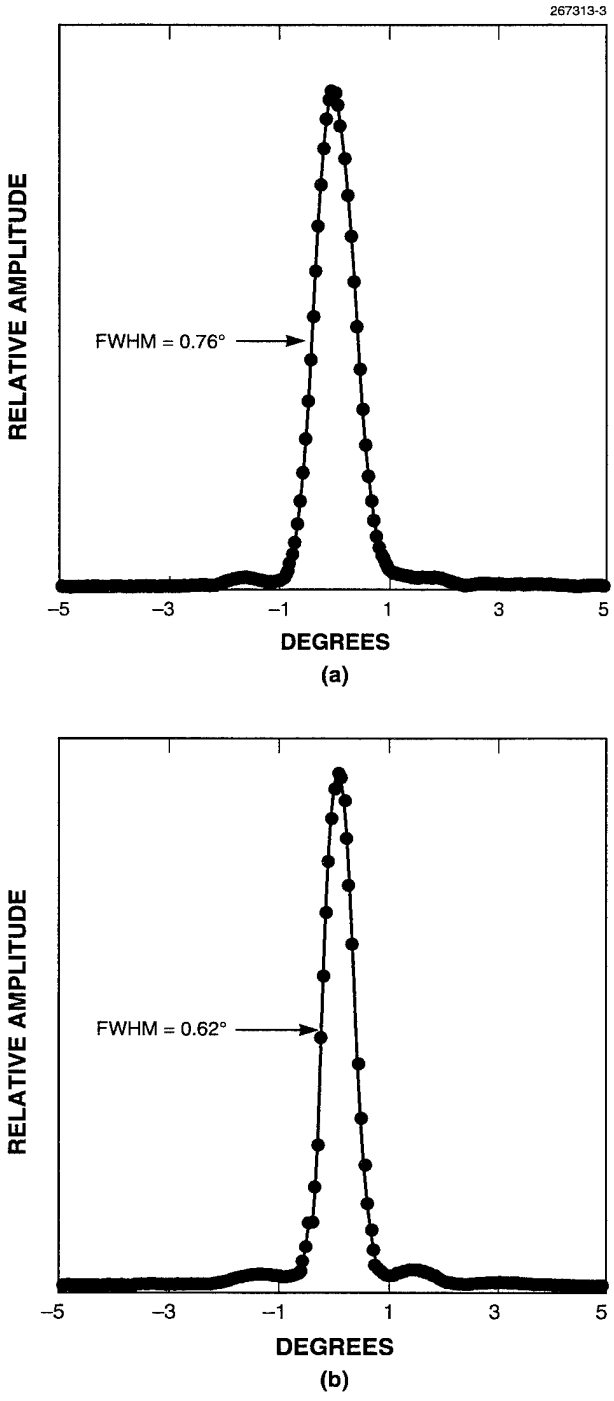

Figure 1-3. Far-field measurement of optical assembly (a) parallel and (b) perpendicular to the laser junction.

This microlens packaging approach, which is very compact and does not require rigid external lens mounts, can reduce the number of independent axes required to align laser arrays and lens arrays in future free-space and fiber-coupled optical systems. The scheme is particularly attractive when large wafers of precise lenses can be manufactured at low cost. Work is currently under way to use the approach to align anamorphic lenses to tapered lasers [3],[4], to show the feasibility of a compact optical assembly with high coupling efficiency to single-mode fiber.

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REFERENCES

1. Z. L. Liau, D. E. Mull, C. L. Dennis, R. C. Williamson, and R. G. Waarts, *Appl. Phys. Lett.* **64**, 1484 (1994).

2. Z. L. Liau, J. N. Walpole, D. E. Mull, C. L. Dennis, and L. J. Missaggia, *Appl. Phys. Lett.* **64**, 3368 (1994).

3. S. H. Groves, J. P. Donnelly, J. N. Walpole, J. D. Woodhouse, L. J. Missaggia, R. J. Bailey, and A. Napoleone, *IEEE Photon. Technol. Lett.* **6**, 1286 (1994).

4. Solid State Research Report, Lincoln Laboratory, MIT, 1994:2, p. 8.

2. QUANTUM ELECTRONICS

2.1 MULTIPASS OPTICAL PARAMETRIC AMPLIFIER

A compact, multipass, optical parametric amplifier (OPA) [1] has been developed for efficient parametric conversion of low-energy, short-duration pump pulses. (The concept of optical parametric amplification is illustrated in Figure 2-1.) Figure 2-2 shows a schematic of the multipass OPA for four passes through the nonlinear crystal. This geometry has the advantage of multiply passing radiation through the nonlinear crystal with the same beam parameters on the final pass as on the initial pass, and therefore a small-diameter beam can be maintained for many passes of the nonlinear crystal. The number of passes through the nonlinear crystal can be controlled by angular adjustment of the flat mirror or by transverse translation of the lens. By eliminating the idler radiation after each pass through the nonlinear crystal, no rephasing of the pump and signal radiation is required and the angular acceptance of the OPA is that of a single pass through the nonlinear crystal. Although elimination of the idler radiation will result in an increase in the threshold pump power, this increase is small and well worth the simplification obtained in the OPA.

By utilizing an amplified passively Q-switched Nd:YAG microlaser [2], an eight-pass OPA has been constructed (same as Figure 2-2, except with eight passes of the nonlinear crystal). A 1.5-cm-long by 0.5-cm-wide by 0.25-cm-high, X-cut KTP crystal was used for noncritical phase matching of the pump (1064 nm), signal (1572 nm), and idler (3293 nm) radiation [3]. The roof prism was constructed from BK7 glass with a base of 0.45 cm, a height of 0.4 cm, and a depth of 0.25 cm. The apex of the prism was polished to provide a 600-μm-width aperture for entry of the 200-μm (e^{-2} intensity) diameter of the

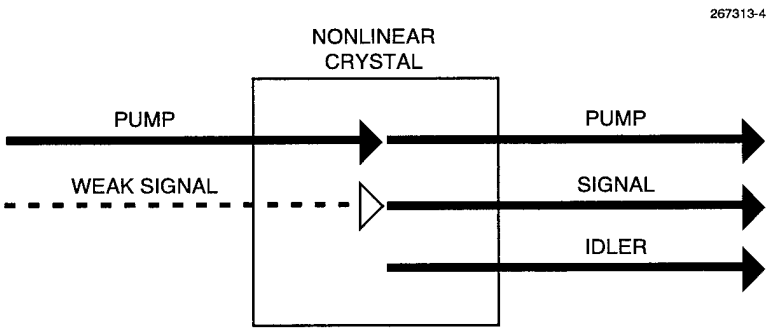

Figure 2-1. Optical parametric amplification of weak signal radiation by strong pump radiation. The pump radiation is converted to both signal and idler radiation. Energy conservation requires that the sum of the signal and idler photon energies is equal to the pump photon energy. The wavelengths of the pump and signal radiation for which there is substantial parametric amplification are determined by the relative orientations of the crystallographic axis, the radiation propagation direction, and the radiation polarization directions. For sufficiently high pump intensity, the gain of the parametric amplifier can be sufficient to amplify the background quantum fluctuations at the signal wavelength so that substantial signal output can be obtained with no intentional signal input.

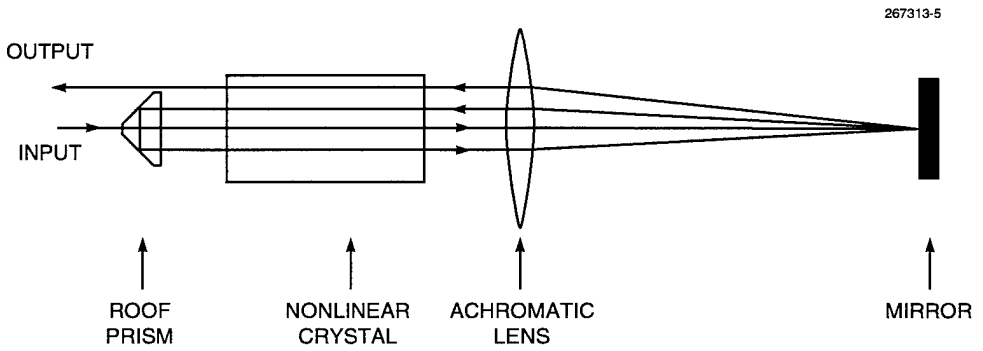

Figure 2-2. Multipass optical parametric amplifier (OPA) showing four passes of the pump radiation through the nonlinear crystal.

pump radiation into the OPA. The apex and total internal reflection surfaces were uncoated, and the base surface was antireflection coated at both 1064 and 1572 nm. A singlet, planoconvex calcium fluoride lens with a nominal focal length of 6 cm was used for relaying the OPA radiation between successive passes of the crystal. The walk-off of the pump and signal radiation after eight passes of the nonlinear crystal due to the difference in focal lengths of the calcium fluoride lens at 1064 and 1572 nm was calculated to be less than 15% of the pump beam diameter. The calcium fluoride lens was antireflection coated at 1064 and 1572 nm. The end mirror was high reflection coated for 1064 and 1572 nm and had a reflectivity of 12% at 3293 nm. KTP has an absorption coefficient [4] of about 0.5 cm^{-1} at 3200 nm, and thus much of the idler radiation is absorbed in the KTP crystal. The BK7 prism absorbed the incident 3293-nm radiation, and the OPA end mirror transmitted most of this radiation. Thus, the OPA was highly lossy for the idler radiation, and rephasing this radiation with the pump and signal beat frequency was not necessary. The overall length of the OPA was 12.6 cm.

With an input pump-pulse duration of 360 ps, an input energy of 150 μJ, an input beam diameter of 200 μm, and eight passes through the KTP crystal, 54% of the output radiation was signal radiation. If the idler radiation is accounted for, this corresponds to a pump depletion of 80%. The OPA had a relatively high transmission loss for the input pump radiation, with only 65% transmission for eight passes of the KTP crystal. The 5% loss per one-way pass of the OPA greatly exceeds what we believe is possible with better optical coatings. Because of pump transmission losses in the OPA, we observed an output signal energy of 30% of the input pump energy. Under these conditions the OPA had a pump threshold of about 52 μJ. By focusing the input pump to a beam diameter of 140 μm the threshold was reduced to 45 μJ. Figure 2-3 shows the energy performance of the OPA. The OPA output energies were measured with a pyroelectric detector after reflecting from an external 1064- and 1572-nm-high reflector. There was no measurable 3293-nm radiation in the output beam. The output signal energy had a linewidth of 1.2 nm, in agreement with phase matching calculations.

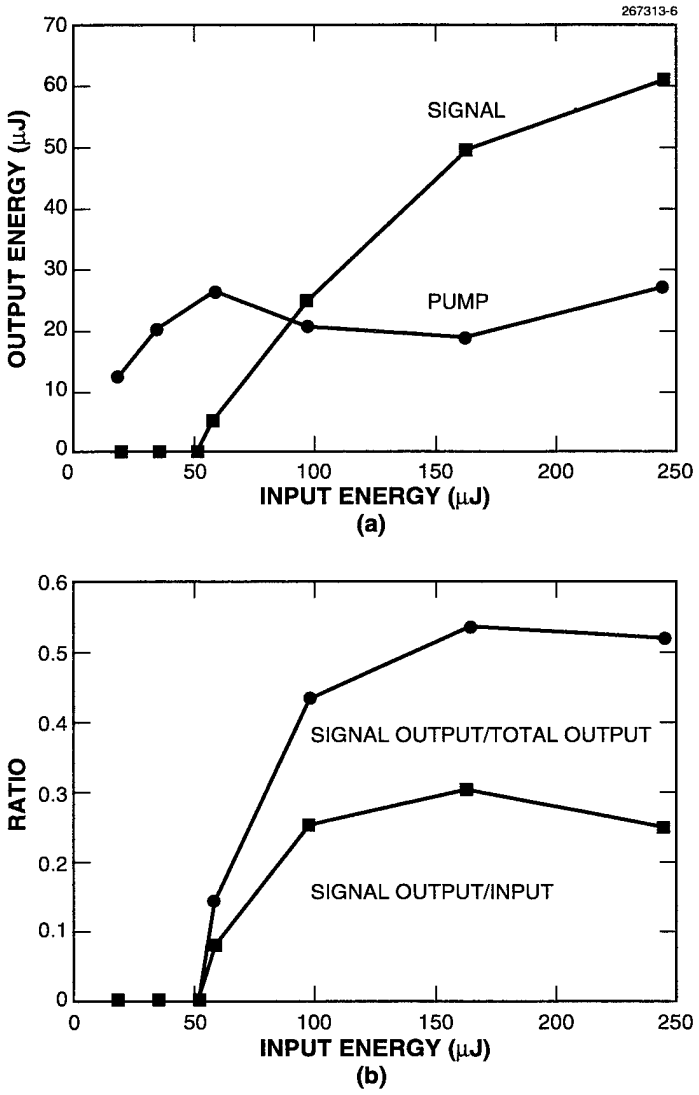

Figure 2-3. (a) Output pulse energies for parametric amplifier in which pump radiation travels through a noncritically phase-matched KTP crystal eight times (twice that shown in Figure 2-2). The signal radiation begins efficient generation at a pump threshold of 52 μJ. (b) Parametric amplification efficiency as a function of input pump (1064 nm) energy. A maximum of 54% of the output radiation was signal (1572 nm) radiation corresponding to 80% pump depletion. Because of OPA coating losses at the pump wavelength, 30% of the input pump energy was converted into output signal energy. The maximum theoretical conversion efficiency of pump radiation to signal radiation is 67%.

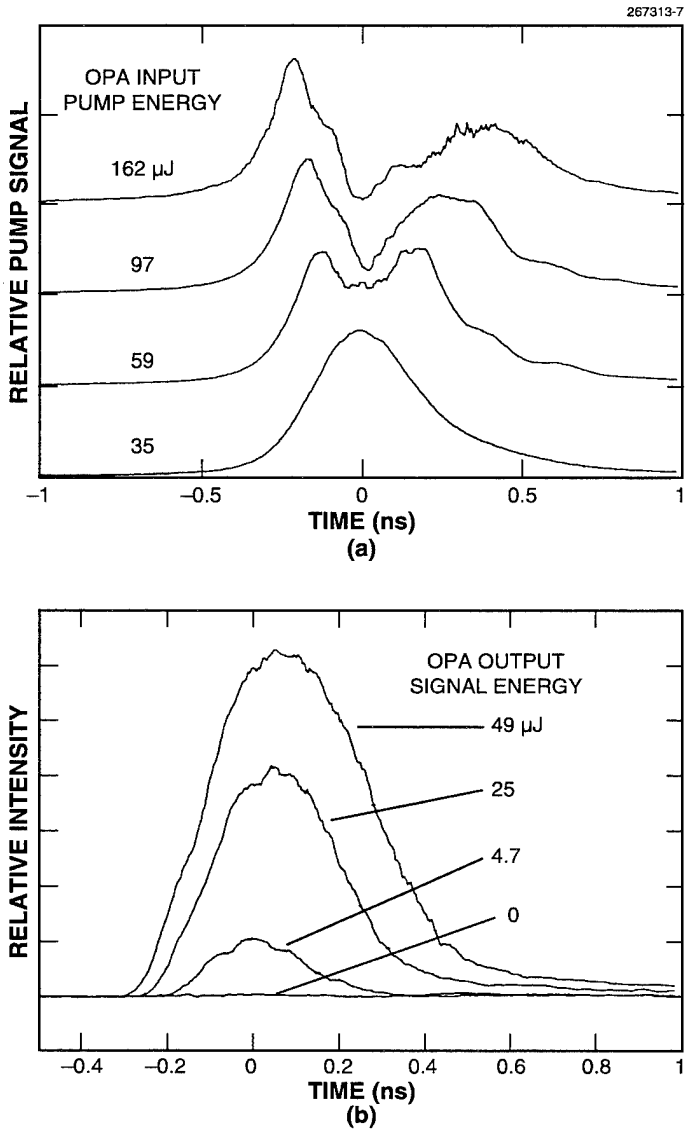

Figure 2-4. (a) Temporal profiles of OPA output pump radiation for various input energies. Above threshold, the pump-pulse profile is dramatically changed because of conversion to signal and idler radiation. (b) Temporal profiles of OPA output signal radiation for various output signal energies corresponding to the pump energies in (a). Near threshold, the signal radiation has a significantly shorter pulse duration than the pump radiation and the signal energy is very sensitive to small changes in the pump energy.

Figure 2-4 shows the temporal profiles of the output pump and signal radiation. The pump radiation was separated from the signal by passing it through a water-filled cell that absorbed all of the signal radiation. The signal radiation was separated from the pump by passing it through a 0.5-cm-thick silicon plate. The temporal pulse shapes were measured with a high-speed (rise time < 35 ps) InGaAsP photodetector and a 20-GHz-bandwidth sampling oscilloscope. As shown in Figure 4(a), the output pump pulse is dramatically changed by the parametric generation. For an input pump energy of 162 μJ, almost all of the pump energy is depleted at t = 0 ns. This illustrates the advantage of the OPA with repeated removal of the idler radiation. The generated signal is centered in time on the center of the pump radiation, and sum-frequency mixing of idler and signal radiation is suppressed so complete depletion of the pump radiation is possible.

We observed optical damage on the first-pass output face of the KTP crystal on two separate occasions with pump energies of 240 and 280 μJ. These energies correspond to intensities of about 1 GW/cm^2.

This technology may have many applications in which short-pulse, low-energy radiation is desired at wavelengths accessible by optical parametric generation. We have developed the technology specifically for the generation of eyesafe 1.57-μm radiation from 1.06-μm Nd:YAG laser radiation for ranging and radar applications.

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REFERENCES

1. R. Baumgartner and R. L. Byer, *IEEE J. Quantum Electron.* **15**, 432 (1979).
2. J. J. Zayhowski and C. Dill III, *Opt. Lett.* **19**, 1429 (1994).
3. L. R. Marshall, J. Kasinski, and R. L. Burnham, *Opt. Lett.* **16**, 1680 (1991); L. R. Marshall, A. Kaz, and R. L. Burnham, *Proc. SPIE* **1627**, 262 (1992).
4. K. Kato, *IEEE J. Quantum Electron.* **15**, 432 (1979); W. M. Theis, G. B. Norris, and M. D. Porter, *Appl. Phys. Lett.* **46**, 1033 (1985); J. M. Breteau, C. Jourdain, T. Lepine, and F. Simon, *OSA Proc. Adv. Solid-State Lasers* **15**, 137 (1993).

3. MATERIALS RESEARCH

3.1 PHOTOELECTROCHEMICAL ETCHING OF MICROLENSES IN SILICON

Procedures for etching arbitrary profiles into the surface of a semiconductor wafer have numerous applications in device processing. Mask-based techniques such as wet-chemical and plasma etching are widely used to produce mesas, trenches, and a variety of other profiles for electronic and optoelectronic devices [1], as well as for sensors and other micromechanical structures [2]. Recently, a growing interest in the utilization of monolithic refractive and diffractive optical elements has stimulated research in applying previously developed etching techniques to the fabrication of such elements on both semiconductor and insulating substrates. However, mask-based techniques generally have serious limitations in forming high-quality optical elements such as microlenses, for which the exact shape of the profile is much more critical than in the case of electronic, optoelectronic, and micromechanical devices. The radius of curvature as well as sidewall depth and slope must be precisely controlled, and spherical symmetry is often necessary to minimize optical aberration. With mask-based etching techniques, where the profile shape is influenced by mask erosion as well as etch selectivity, such exacting control is difficult. Precise control of profile shape is also difficult with other mask-based processes such as photoresist reflow [3] and mass transport [4]. A disadvantage with all mask-based techniques is the requirement to form a suitable mask on the surface to be etched. This usually requires coating the surface with photoresist material, lithography, and photoresist removal. Although these processes are well developed, nonplanar surfaces or ultraclean surfaces are often difficult to deal with.

Photoelectrochemical etching has been shown to be an excellent maskless technique for the etching of microlenses and other optical structures into the surface of III-V wafers, using lamp [5],[6] as well as scanned laser illumination [7]. In photoelectrochemical etching the wafer to be etched is made to be one electrode in a suitable electrochemical bath, and an external potential is applied between the wafer surface and an appropriate counter electrode. Spatial variation in the illumination of the wafer surface/electrolyte interface is used to control the local etch rate. The incident light controls the etch rate by providing the necessary carrier type (either electrons or holes, depending on the polarity of the wafer and the applied potential) to permit an otherwise limited oxidation/reduction reaction to proceed. Control of the maximum etch rate is also provided by varying the applied voltage and current to the electrochemical cell. While photoelectrochemical etching of III-V materials has been well demonstrated, this technique has not been widely applied to the etching of Si, primarily because of the tendency of Si to form an insoluble oxide at the semiconductor/electrolyte interface which interferes with a continuing oxidation/reduction reaction.

The results presented here are based on our observation that a NaF/H_2SO_4-based Si etch previously developed for uniform etching during capacitance-voltage (C-V) carrier profiling of Si [8], and also used as an electrolyte in a commercial C-V profiling system [9], has excellent linearity of etch rate as a function of light intensity and is capable of producing smooth etched surfaces. With this electrolyte chemistry, combined with a suitable method for varying the illumination intensity on the surface of the wafer, we have found that a wide variety of profiles can be produced in the surface of a Si wafer.

For our experiments, we used starting procedures similar to those previously reported [8]. Sufficient NaF powder was added to a 0.05M H_2SO_4/H_2O starting solution to make a 1M NaF solution. This

solution was mixed with deionized water and a surface wetting agent (Triton X-100) in a ratio of 100:200:1. We assume a standard anodic chemistry

$$Si + 2h^+ \rightarrow Si^{2+} \tag{3.1}$$

with the accompanying oxidation reduction reaction

$$Si^{2+} + 2(OH)^- \rightarrow Si(OH)_2$$

$$Si(OH)_2 \rightarrow SiO_2 + H_2 \ . \tag{3.2}$$

We used 10–30-Ω cm *n*-type Si wafers, dipped in a buffered HF solution for initial oxide removal, and a Pt counter electrode. Experiments employing constant voltage and constant current were performed, but our best results were produced using constant voltage conditions. Unlike the previous work for C-V profiling, which used uniform illumination, we needed to develop a technique to produce a controlled variation of light intensity across the wafer surface. To do this we started with a desktop-computer-generated pattern, comprising a two-dimensional array of circles made up of concentric annular rings, with each ring having a different dot density. The densities of dots in the annular rings were chosen to approximate a parabolic variation of intensity with radius. The image of these circles was photographically reduced and a defocused version was produced on a 35-mm film negative in the format of a conventional 2 × 2-in. slide. The defocusing allowed blurring of the individual dot patterns into a more smoothly varying change of transmitted intensity with radius.

As shown in the schematic of the experimental arrangement of Figure 3-1, the image of the slide was then projected through the electrolyte onto the wafer surface by using a fiber-optic illuminator, a collimating lens, and a microscope objective, producing an additional reduction in the image size. From calibrated detector measurements we estimate that the maximum illumination intensities on the wafer surface were between 10 and 100 mW/cm^2 during etching. With an applied voltage of 2 V, maximum illuminated etch rates of ~ 0.7 μm/h were obtained, with smoothly etched surfaces. The profile of one of the individual microlenses was measured by the use of a scanning surface profilometer. We also measured the transmission profile of the actual dot pattern on the 2 × 2-in. slide by scanning a focused laser spot across the region on the slide containing a single dot, with a detector placed behind the slide to measure the transmitted intensity. Figure 3-2 shows a comparison of the etched profile with the normalized transmission profile, demonstrating excellent linearity of the etch rate vs illumination level. Figure 3-3 shows a microphotograph of the transmission of the infrared image of the letter *A* through the Si wafer with the focusing optical effect of the microlens array clearly visible.

The photoelectrochemical etching technique that we have demonstrated is capable of producing almost arbitrary profiles on the surface of a Si wafer. This technique may prove useful for the fabrication of microlenses and other structures in Si where precise control of etch profile is required.

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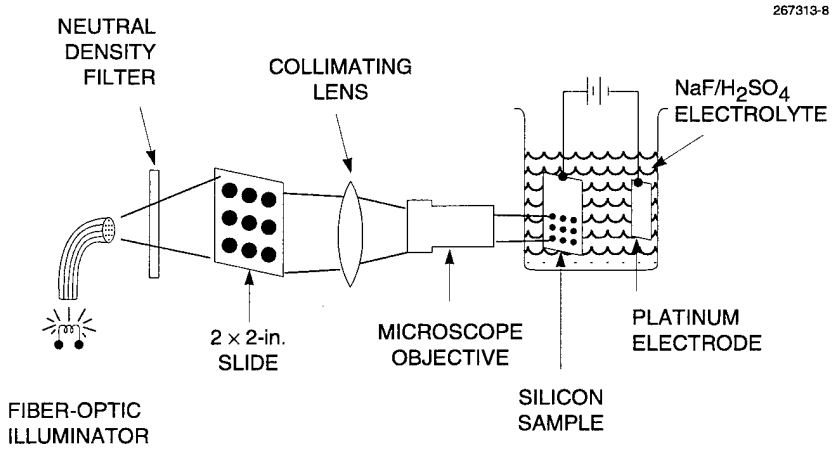

Figure 3-1. Schematic diagram of photoelectrochemical etching apparatus.

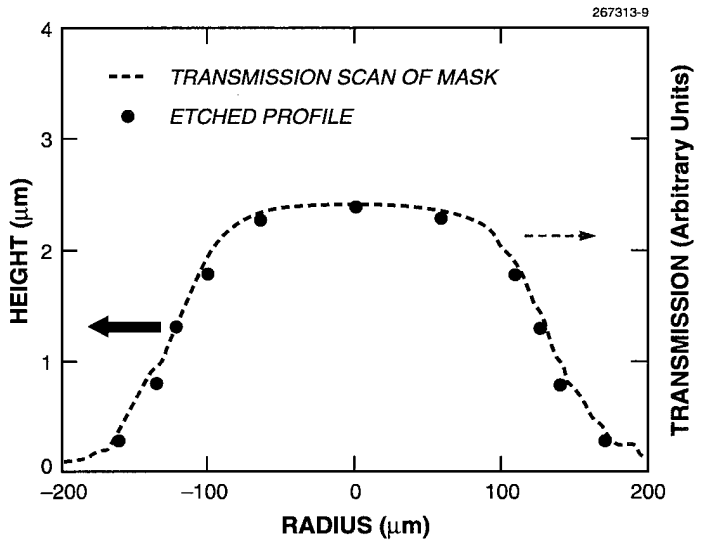

Figure 3-2. Comparison of photoelectrochemically etched profile with transmission scan of projected mask.

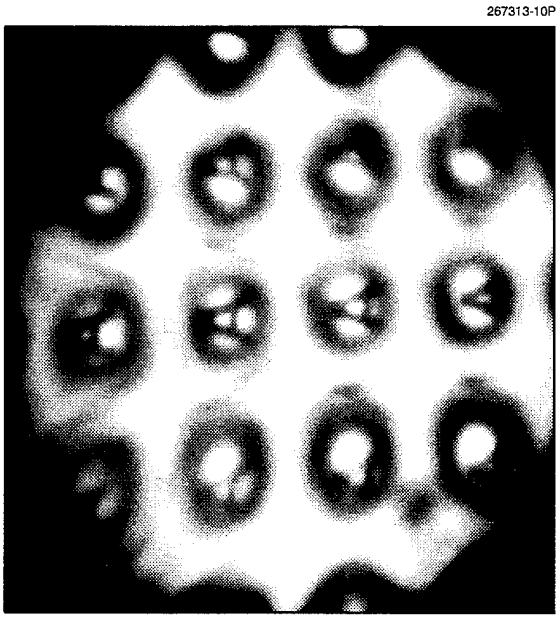

Figure 3-3. Photomicrograph of transmitted infrared image through Si wafer with microlens array.

3.2 LOW CARBON AND OXYGEN IN AlGaAs GROWN WITH TRITERTIARYBUTYLALUMINUM

The reduction of oxygen and carbon in AlGaAs alloys can ultimately lead to improved performance for electronic and optoelectronic devices. Oxygen can deleteriously affect the optical and electrical properties, and carbon can compensate intentional donor impurities. Oxygen and carbon are typically observed in layers grown by organometallic vapor phase epitaxy (OMVPE) with the conventional methyl-based precursors trimethylaluminum (TMAl) and trimethylgallium (TMGa). Oxygen incorporation in AlGaAs can be reduced by increasing growth temperatures [10], and numerous studies report carbon reduction through the use of triethylaluminum [11] or Al-hydride adduct compounds [12]–[14] in conjunction with triethylgallium (TEGa). Recently, we reported use of the novel aluminum precursor tritertiarybutylaluminum (TTBAl) for OMVPE growth of AlGaSb layers [15]. Here, we report the use of TTBAl in conjunction with TEGa for growth of high-quality AlGaAs layers.

AlGaAs layers were grown on semi-insulating or n^+ (100) GaAs substrates, misoriented 2° toward (110), in a vertical rotating-disk reactor operated at 150 Torr with a H_2 carrier gas flow rate of 10 slpm. The source precursors were TTBAl, TEGa, and 100% AsH_3. TEGa was an oxygen-reduced grade, and the AsH_3 was passed through a purifier to remove O_2 and H_2O. The layers were grown at 650°C, which is a relatively low temperature for AlGaAs grown by OMVPE. The ratio of TTBAl to the total group III input ranged from 0.2 to 0.8, and the V/III ratio was kept constant at 70. The AlGaAs epilayers were capped with a thin (~ 5 nm) GaAs layer to facilitate ohmic contact formation.

The surface morphology was examined using Nomarski contrast microscopy. The alloy composition of AlGaAs layers was determined from photoluminescence (PL) spectra measured at 4 K [16] or by double-crystal x-ray diffraction (DCXD) [17]. Pendellosung fringes in DCXD scans were used to evaluate layer thickness for determining growth rates. The background concentration was determined from C-V and Hall measurements. Secondary ion mass spectroscopy (SIMS) was used to obtain C, O, and Si concentrations.

Figure 3-4 shows the dependence of AlAs content in $Al_xGa_{1-x}As$ layers on TTBAl concentration in the gas phase. AlAs incorporation is only about 50% efficient. The growth rate of $Al_{0.1}Ga_{0.9}As$ was 1.8 Å/s for a total group III input of 1×10^{-4} mole fraction, and decreased to 0.7 Å/s for $Al_{0.5}Ga_{0.5}As$. The reduction in growth rate and AlAs incorporation could not be correlated with source prereaction since in situ concentration monitoring using fiber-optic-based Fourier transform infrared spectroscopy indicated minimal interaction between TTBAl and AsH_3 [18]. A more likely explanation may be related to steric effects, which cause an unusually low surface sticking coefficient [19]–[20]. The surface morphology of all layers grown in this study with $0.1 \leq x \leq 0.5$ exhibited a smooth mirror and featureless morphology. This result is in contrast with our experience for low-temperature (650–700°C) growth of AlGaAs layers from TMAl and TMGa or trimethylaminealane (or dimethylethylaminealane) and TEGa. Typically those surfaces were mirror but contained numerous defects.

Strong room-temperature PL was observed for samples with direct band gaps. The low-temperature PL spectrum from an $Al_{0.26}Ga_{0.74}As$ layer is shown in Figure 3-5 and is dominated by the bound exciton (BE) transition. The band-to-acceptor transition that is typically observed at 24-meV lower energy than BE is absent, and no evidence for recombination due to carbon impurities is indicated. The full width at half-maximum of the BE transition is 5.6 meV, which compares favorably with high-purity AlGaAs [21].

SIMS analysis for C, O, and Si in an AlGaAs multilayer structure consisting of $Al_{0.25}Ga_{0.75}As$, $Al_{0.2}Ga_{0.8}As$, and $Al_{0.1}Ga_{0.9}As$ is shown in Figure 3-6. Carbon is not detectable at the SIMS limit of $\sim 10^{16}$ cm^{-3} in any of the layers, while O is at a concentration of $2–3 \times 10^{17}$ cm^{-3}, which is slightly higher than the detection limit of $1–2 \times 10^{17}$ cm^{-3}. The O level is unusually low for AlGaAs layers grown at the low temperature of 650°C, compared to more typical values of 8×10^{17} cm^{-3}, which were measured in layers grown with TMAl and TMGa [10]. With these precursors the low levels could only be obtained for AlGaAs layers grown in our reactor at the high temperature of 800°C. Silicon is below the detectable level of $\sim 2–4 \times 10^{16}$ cm^{-3}, the lower limit as a result of mass interference of AlH with Si.

All $Al_xGa_{1-x}As$ layers grown in this study, $0.1 \leq x \leq 0.5$, exhibited *n*-type conductivity with a carrier concentration at $\sim 1.0–1.5 \times 10^{16}$ cm^{-3}, which was invariant of *x*-value. This result is consistent with the low carbon levels and indicates minimal metal impurities in the TTBAl source. Hall measurements were compromised by two-dimensional electron gas effects that were observed as a doping spike at the epilayer-substrate interface in C-V profiles, especially for samples with $x \geq 0.2$. This effect is expected to be minimal in the $Al_{0.1}Ga_{0.9}As$ layer, for which the doping spike was absent. The room-temperature and 77-K mobilities for this sample were 4.3×10^3 and 10^4 cm^2/V s, respectively.

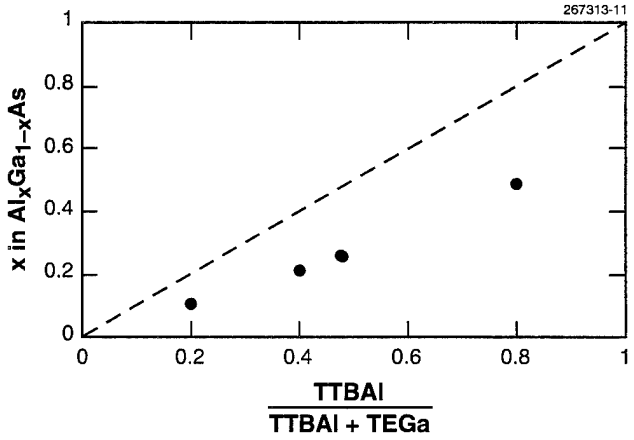

Figure 3-4. Dependence of AlAs solid composition on TTBAl concentration in the gas phase.

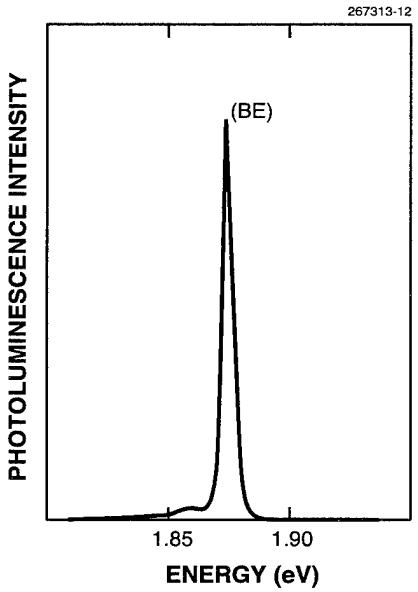

Figure 3-5. Photoluminescence spectra at 4 K of $Al_xGa_{1-x}As$ layers grown with TTBAl and TEGa.

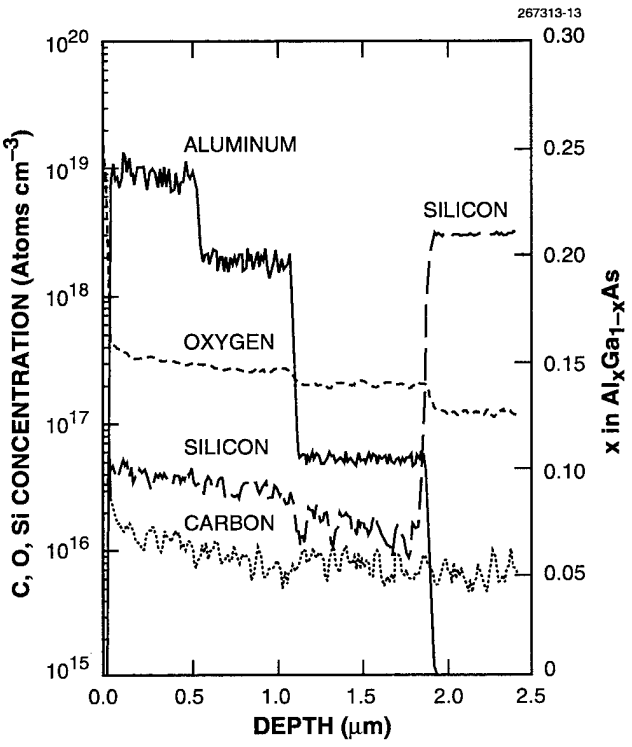

Figure 3-6. Secondary ion mass spectroscopy profiles of C, O, Si, and Al in AlGaAs multilayer structure grown with TTBAl and TEGa.

For ternary alloys grown with sources that decompose at relatively low temperatures, source prereactions and premature decomposition can deleteriously affect compositional uniformity. No such difficulties were encountered with TTBAl. The AlGaAs uniformity over a 5-cm-diam substrate was evaluated by determining the composition along the diameter of the substrate by room-temperature PL spectra. Since the wafer is rotated at 450 rpm, composition is expected to be radially symmetric. For $Al_xGa_{1-x}As$ with an average x-value of 0.268, the standard deviation was only 0.001. This high uniformity indicates the suitability of TTBAl with TEGa and AsH_3 for $Al_xGa_{1-x}As$ epitaxy.

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REFERENCES

1. S. K. Ghandi, *VLSI Fabrication Principles* (Wiley, New York, 1983), p. 475.
2. *Proceedings of the IEEE Micro Electro Mechanical Systems Conference* (IEEE, New York, 1991).
3. Y. Sano, T. Nomura, H. Aoki, S. Terakawa, H. Kodama, T. Aoki, Y. Hiroshima, *Proceedings of the 1990 IEEE International Electron Devices Meeting* (IEEE, New York, 1990), p. 283.
4. Z. L. Liau and J. N. Walpole, *Appl. Phys. Lett.* **50**, 528 (1987).
5. F. W. Ostermayer, Jr., P. A. Kohl, and R. H. Burton, *Appl. Phys. Lett.* **43**, 642 (1983).
6. P. A. Kohl and F. W. Ostermayer, Jr., *Ann. Rev. Mater. Sci.* **19**, 379 (1989).
7. M. N. Ruberto, X. Zhang, R. Scarmozzino, A. E. Willner, D. V. Podlesnik, and R. M. Osgood, Jr., *J. Electrochem. Soc.* **138**, 1174 (1991).
8. W. Y. Leong, R. A. A. Kubiak, and E. H. C. Parker, *Proceedings of the First Symposium on Si MBE* (Electrochemical Society, Pennington, N.J., 1985), p. 140.
9. Bio-Rad Micromeasurements Division, Mountain View, Calif.
10. T. F. Kuech, R. Potemski, F. Cardone, and G. Scilla, *J. Electron. Mater.* **21**, 341 (1992).
11. N. Kobayashi and T. Makimoto, *Jpn. J. Appl. Phys.* **24**, L824 (1985).
12. A. C. Jones and S. A. Rushworth, *J. Cryst. Growth* **106**, 253 (1990).
13. W. S. Hobson, T. D. Harris, C. R. Abernathy, and S. J. Pearton, *Appl. Phys. Lett.* **58**, 77 (1991).
14. S. M. Olsthoorn, F. A. J. M. Driessen, L. J. Giling, D. M. Frigo, and C. J. Smit, *Appl. Phys. Lett.* **60**, 82 (1992).
15. C. A. Wang, M. C. Finn, S. Salim, K. F. Jensen, and A. C. Jones, *Appl. Phys. Lett.* **67**, 1384 (1995).
16. T. F. Kuech, D. J. Wolford, R. Potemski, J. A. Bradley, K. H. Kelleher, D. Yan, J. P. Farrell, P. M. S. Lesser, and F. H. Pollack, *Appl. Phys. Lett.* **57**, 505 (1987).
17. B. K. Tanner, A. G. Turnbull, C. R. Stanley, A. H. Kean, and M. McElhinney, *Appl. Phys. Lett.* **59**, 2272 (1991).
18. S. Salim, Ph.D. thesis, Massachusetts Institute of Technology, 1995.
19. J. S. Foord, N. K. Singh, E. T. FitzGerald, G. J. Davies, and A. C. Jones, *J. Cryst. Growth* **120**, 103 (1992).
20. B. Willis and K. F. Jensen, private communication.
21. T. F. Kuech, D. J. Wolford, E. Veuhoff, V. Deline, P. M. Mooney, R. Potemski, and J. Bradley, *J. Appl. Phys.* **62**, 632 (1987).

4. SUBMICROMETER TECHNOLOGY

4.1 PLASMA ETCHING OF SUB-0.25-μm POLYSILICON FEATURES PATTERNED WITH SILYLATED RESIST AND 193-nm OPTICAL LITHOGRAPHY

Single-layer resists have been traditionally used in optical lithography, but as resolution requirements approach 0.25 μm and below, advanced techniques such as top-surface imaging (TSI) may become necessary to achieve the required feature size control and process latitude. The TSI process is insensitive to underlying topography and provides increased focus latitude and etch resistance [1].

A positive-tone TSI resist system, illustrated in Figure 4-1, has been designed for use with 193-nm lithography [2],[3]. The process is based on the use of a polyvinylphenol (PVP) resist, which becomes selectively crosslinked when exposed to 193-nm radiation. The substrate is then treated with a silicon-containing vapor, dimethylsilyldimethylamine, at a temperature of 90°C and a pressure of 25 Torr for 30 to 75 s. The uncrosslinked PVP areas incorporate a controlled amount of silicon, whereas the crosslinked areas do not. The wafers are then dry developed in a high-ion-density helicon plasma etcher in an oxygen-based plasma [4]. The oxygen reacts with the silylated areas to form SiO_2, which acts as an etch mask in the unexposed areas. The silylation and etching parameters have been optimized to maximize uniformity, feature size control, feature size linearity, and process latitude [5].

In this report, we describe the optimization of the plasma etching of polysilicon using this TSI process. The goal is to produce vertical profiles for sub-0.25-μm-wide features with good resist and oxide selectivity, while maintaining good process latitude, high throughput, good uniformity, and linearity between different feature types.

Three different sets of experiments were used to study etch rates, pattern dependencies, and etch profiles. All of the experiments used the high-ion-density helicon plasma etcher. Unpatterned wafers consisting of an ~ 1-μm-thick layer of novolac resist, and 3000–6000 Å of undoped polysilicon on 50–1000 Å of SiO_2 were used to optimize the etching parameters. Source power, chuck power, flow rate, gas chemistry, temperature, and pressure were adjusted to obtain etch rates > 3000 Å/min (for polysilicon), selectivity > 2:1 (for resist), high selectivity to oxide (> 200:1), and nonuniformity < 3% (3σ). An in situ imaging interferometry system was used, which greatly reduces process development time [6]. Wafers consisting of 3000 Å of undoped polysilicon on 50 Å of SiO_2 and patterned with i-line lithography were used to optimize etched profiles and check selectivities as a function of wafer resist coverage. Finally, wafers patterned with 193-nm lithography consisting of 3000 Å of polysilicon on 50 Å of SiO_2 were used to optimize polysilicon profiles using the silylated PVP resist as the etch mask.

A three-step etch process was developed. Table 4-1 lists the typical etch process conditions and etch results. A high-chuck-power (100 W), 3-s chlorine etch was used to completely remove the native oxide on top of the polysilicon layer. The main etch chemistry was optimized for high polysilicon-to-resist selectivity. Figure 4-2(a) shows the dependence of polysilicon and resist etch rate on percent HBr, while Figure 4-2(b) plots the resulting polysilicon-to-resist selectivity. HBr decreases the resist erosion rate compared to chlorine chemistry. This is attributed to the lower reactivity of Br atoms on the resist surface. By optimizing the HBr/Cl_2 flow ratio, the polysilicon/resist selectivity was improved twofold. In

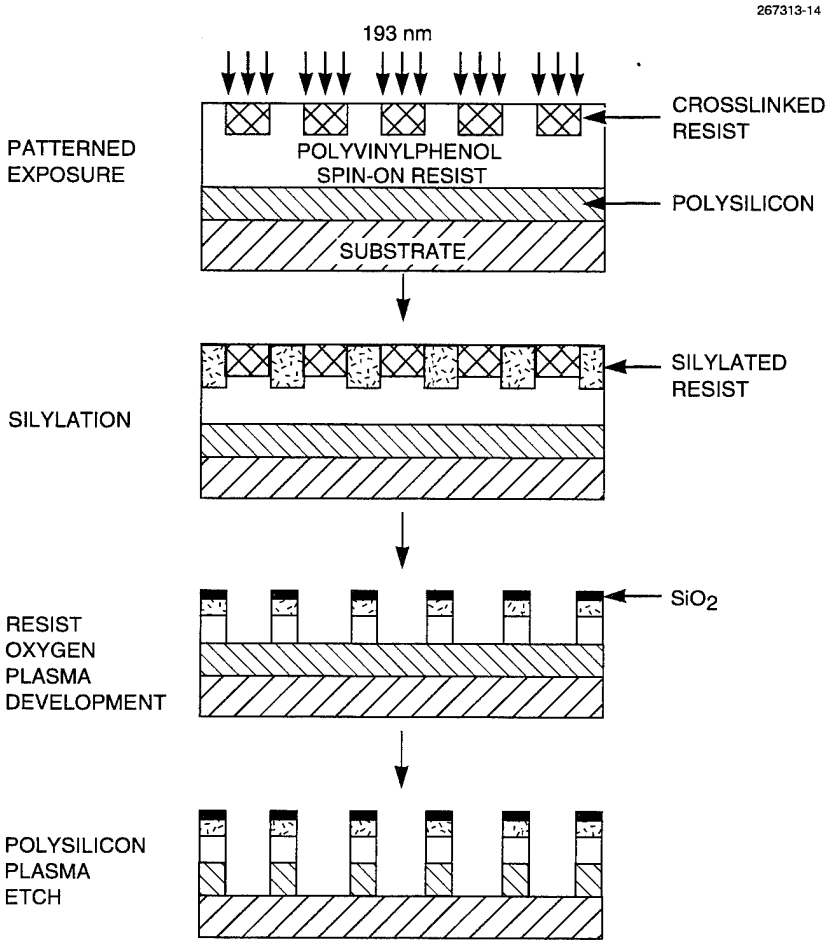

Figure 4-1. Positive-tone 193-nm silylation resist process flow for pattern transfer into polysilicon.

TABLE 4-1

Typical Top-Surface Imaging Process Conditions and Experimental Results Using the Helicon Etcher

	Oxide Removal (Cl_2)	Main Etch (HBr,Cl_2)	Overetch (HBr/O_2)
Process Conditions			
Pressure (mTorr)	2.0	2.0	2.0
Source power (W)	2000	2000	2000
Chuck power (W)	100	50	25
Total flow (sccm) Cl_2 and HBr	50	75	50
100% HBr	0	67	100
O_2 flow (sccm)	—	—	2
Chuck temperature	0°C	0°C	0°C
Etch Results			
Etch uniformity (%) (3σ)	—	3–4	3–4
Poly/resist selectivity	—	2/1–3/1	2/1
Poly/oxide selectivity	—	30/1	>500/1

the overetch step, the use of lower chuck power reduces the oxide etch rate by a factor of 2 (650–350 Å/min), thereby increasing the selectivity by a factor of 2 (6:1–11:1) in pure Cl_2 chemistry, as plotted in Figure 4-3. This is because oxide etching requires more ion bombardment energy, because of the much higher silicon-oxygen bond energy (193 kcal/mol) compared to the silicon-silicon bond energy (78 kcal/mol). By going to HBr at low chuck power the oxide etch rate is reduced even further. In addition, a small amount of oxygen was added in the overetch step. This oxygen significantly diminished the oxide etch rate while the polysilicon rate remained high. Figure 4-4 shows oxide etch rate and polysilicon-to-oxide selectivity as a function of oxygen flow rate. The suppression of oxide etch rate is probably due to surface oxidation.

Overall, reducing chuck power, using HBr chemistry, and adding O_2 dramatically retards the oxide etch rate and minimizes oxide loss to < 10 Å for a 100% overetch, which is critical when etching polysilicon gates with a 50-Å gate oxide layer. This etch process is suitable for stringer removal. Furthermore, this chemistry is highly anisotropic. Figure 4-5 shows some examples of polysilicon features patterned using 193-nm lithography and a silylated etch mask. Vertical and notchless polysilicon profiles were achieved on a 50-Å gate oxide with 500:1 polysilicon-to-oxide selectivity.

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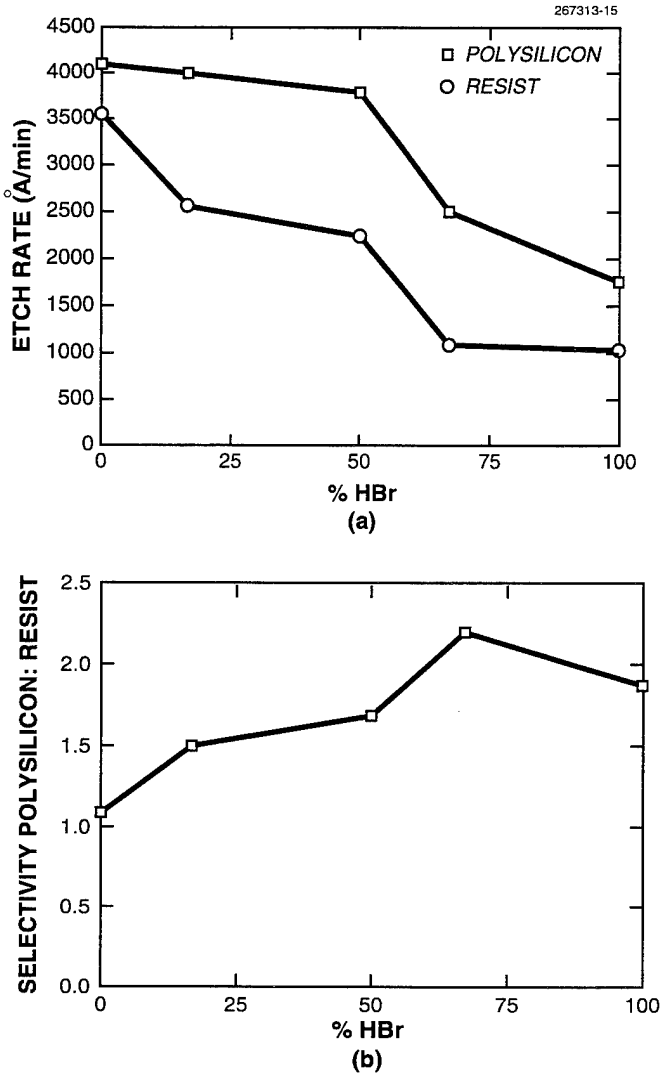

Figure 4-2. (a) Dependence of polysilicon and resist etch rate on percent HBr measured on i-line-patterned wafers for the main etch step. Process conditions are described in Table 4-1, except that the total gas flow (HBr and Cl_2) has been reduced to 50 sccm and the percent HBr is varied as indicated. (b) Polysilicon-to-resist selectivity for same conditions as in (a).

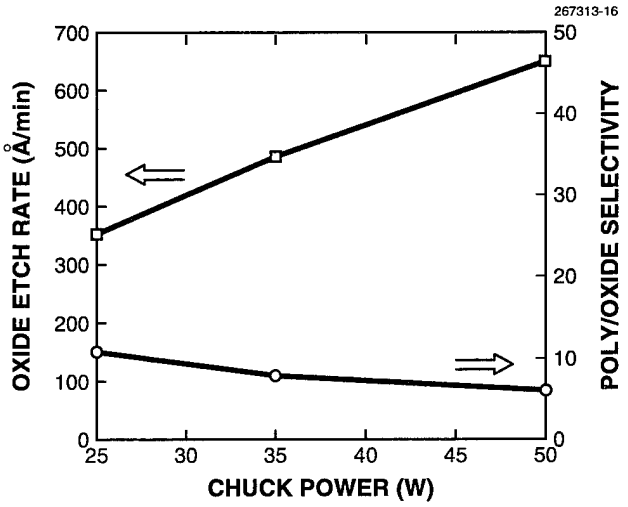

Figure 4-3. Oxide etch rate and polysilicon-to-oxide selectivity vs chuck power. Etch parameters are 2-kW source power, 2-mTorr pressure, 50-sccm Cl_2, and 0° chuck temperature.

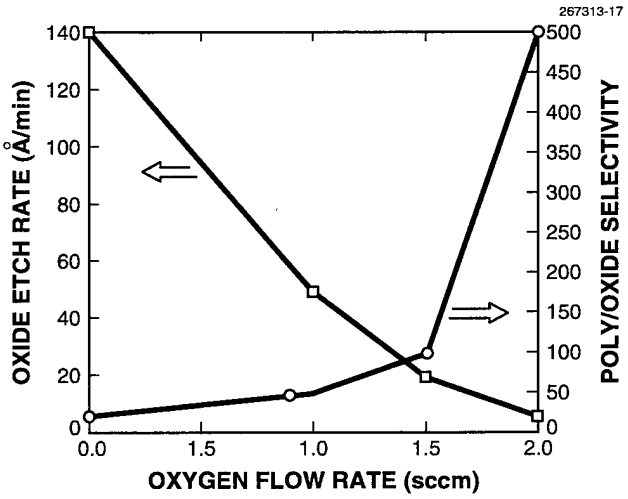

Figure 4-4. Oxide etch rate and polysilicon-to-oxide selectivity vs oxygen flow rate for the overetch step. Process conditions are described in Table 4-1, except the oxygen flow rate is varied as indicated.

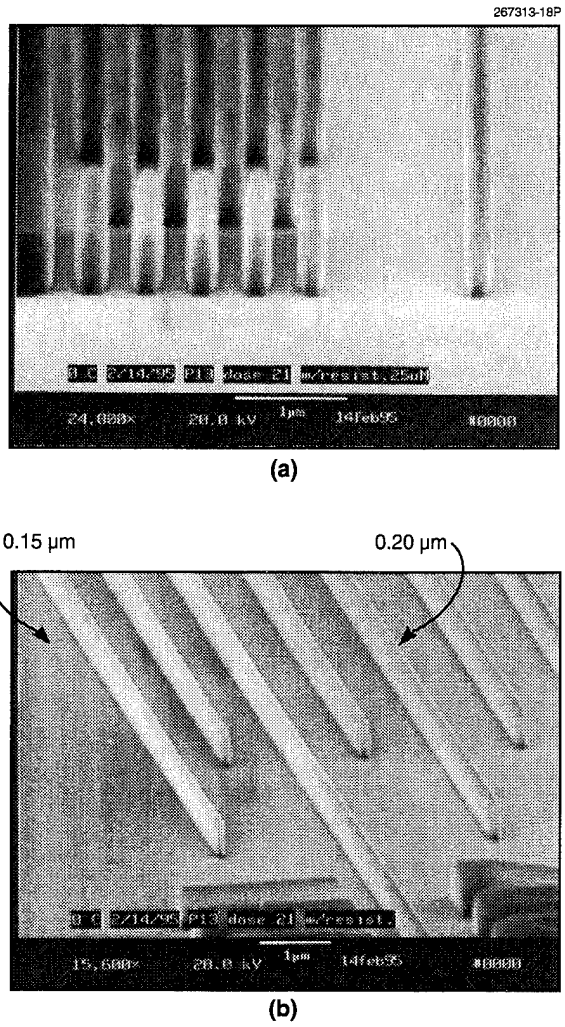

Figure 4-5. Polysilicon features patterned using 193-nm 0.5-numerical-aperture optical stepper, silylated polyvinylphenol resist etch mask, and three-step polysilicon plasma etch process: (a) 0.25-μm equal line and space features and (b) 0.15- and 0.20-μm isolated features.

4.2 OBSERVATION OF A NANOCRYSTALLINE-TO-AMORPHOUS PHASE TRANSITION IN LUMINESCENT POROUS SILICON

We have used valence band x-ray photoelectron spectroscopy (XPS) to probe the electronic structure of porous silicon (po-Si) and to assist in determining its morphology. Since the valence band electronic structure for amorphous silicon (a-Si) and crystalline silicon (c-Si) are clearly different, we can use this technique to look for evidence of nanocrystalline porous silicon (nc-po-Si) within the sampling

depth (~ 10 nm) of XPS, by simply looking for linear combinations of the spectra for amorphous and crystalline phases. The XPS results were confirmed using cross-sectional transmission electron microscopy (XTEM). We are particularly interested in the structure of the near-surface region where the visible photoluminescence (PL) originates.

The wafers used were lightly doped *p*-type Si(100) with 7–25-Ω cm resistivity. The po-Si was prepared using anodic etching in deionized water and HF (1:1). The samples were prepared in a current-limited mode at typical current densities of 100–400 mA/cm^2 and etch times of 1–15 min. After preparation, both XPS survey spectra and Fourier-transform infrared (FTIR) transmission spectroscopy reveal only silyl hydrides on the surface with little or no oxygen or carbon present. This is the expected hydrogen-terminated surface resulting from HF-cleaned Si [7]. The FTIR results yield peaks at 2088, 2110, and 2140 cm^{-1}, indicating the presence of SiH, SiH_2, and SiH_3, respectively, in accordance with previous reports for anodically etched silicon [8].

Figure 4-6 shows the XPS survey spectra of a sample etched for 1 min (two passes in and out of the solution at a speed of 1 mm/s) at an average current density of 100 mA/cm^2, indicating only a trace of fluorine, oxygen, and carbon present in addition to the Si and H. The valence band photoemission spectra are shown in Figure 4-7 for a similar po-Si sample after exposure to a Mg-anode x-ray source (Physical Electronics) at a distance of ~ 1 cm for ~ 30 min (curve b) and ~ 600 min (curve c), along with that for crystalline silicon (curve a). The valence band spectrum for crystalline silicon shows peaks at 3.3, 7.6, and 10.1 eV. The spectrum for crystalline silicon shows good agreement with previous XPS [9] and ultraviolet photoelectron spectroscopy [10] measurements and also with theoretical calculation of silicon's valence band density of states [11]. The spectra for po-Si roughly agree with previous measurements [12], except for a relatively small difference between the sample exposed to x-rays for 600 min vs that exposed for 30 min. The sample exposed for only 30 min shows more crystalline character than fully amorphized silicon [9], indicated by the more pronounced peaks at 7.6 and 10.3 eV. The presence of these peaks is suggestive of a mixed phase of crystalline and amorphous silicon located 0 to ~ 10 nm from the surface. After irradiation for 600 min, the sample surface region appears to have become completely amorphous. In contrast, porous silicon samples prepared using etch times of 10 min all showed valence band XPS signatures similar to those shown in Figure 4-7 (curve c) and reported in Ref. 12, suggesting that longer etch times render the surface few nanometers nearly completely amorphous.

To further confirm the presence of a mixed-phase po-Si in the as-prepared samples, high-resolution XTEM was performed, and the results are shown in Figure 4-8. Figure 4-8(a) shows a high-resolution image of the po-Si/silicon interface demonstrating nanocrystalline inclusions in the range 2–5 nm, whereas Figure 4-8(b) shows a high-resolution image of the surface of the po-Si at the epoxy/po-Si interface. These XTEM results confirm the existence of nanocrystallites small enough for quantum confinement [13] near the surface of the porous silicon, thereby supporting our XPS observations. Interestingly, the XTEM images in Figures 4-8(a) and 4-8(b) were obtained on po-Si samples that were etched for 10 min and which showed no crystalline structure in the valence band XPS. This result further illustrates the fact that XPS only provides average compositional information over a large (1 mm square) area and is relatively insensitive to minor inclusions of crystalline material.

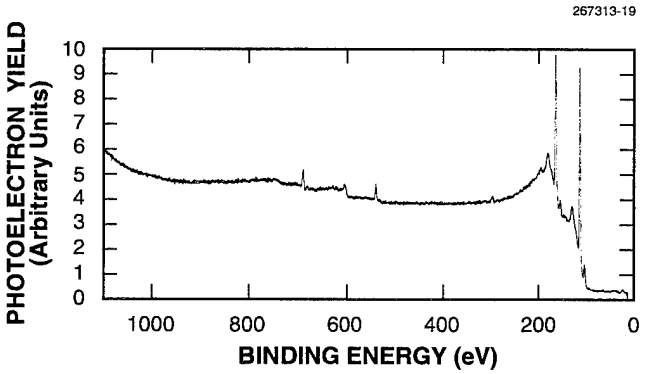

Figure 4-6. Survey x-ray photoelectron spectra (XPS) of anodically etched porous silicon (po-Si). Other than Si, only traces of fluorine, carbon, and oxygen are present. The carbon and oxygen are present because of exposure to air.

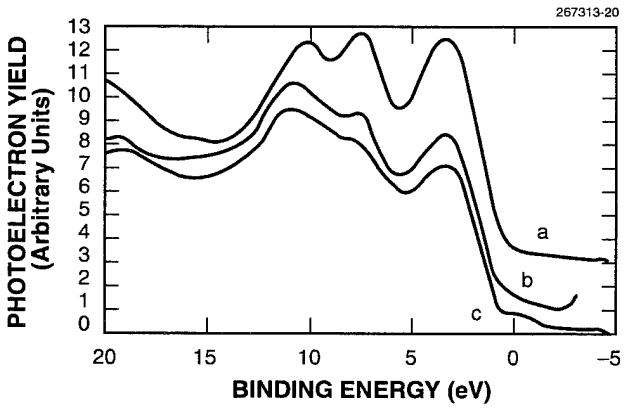

Figure 4-7. Valence band XPS spectra for crystalline Si (curve a), po-Si (curve b), and the same po-Si sample as for curve b but exposed to x-rays for ~ 600 min (curve c). The small peak in curve c near the Fermi edge is a smoothing artifact.

The samples exposed to high doses of x-rays in this study, seen in Figure 4-7 (curve c), were subsequently excited either by 254- or 193-nm radiation, and the resultant PL was compared to that of virgin po-Si. The x-ray-exposed sample exhibited significantly reduced (~ 10–100) luminescence yield, while the area of the sample that was masked by the mounting clip in the XPS still exhibited full-intensity luminescence. This result is in accordance with a reduction in concentration of nanocrystalline silicon phases within the surface 10 nm (the approximate penetration depth of the 193-nm radiation and the

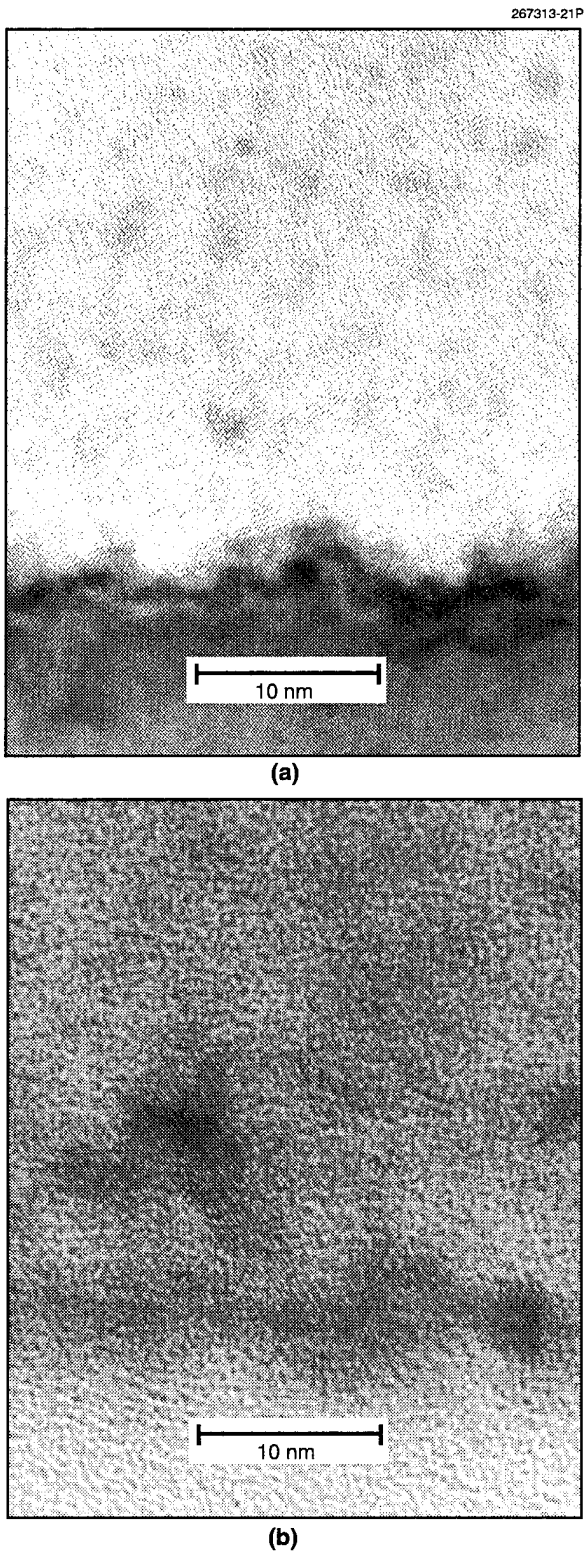

Figure 4-8. (a) High-resolution cross-sectional transmission electron microscopy (XTEM) image of po-Si/silicon interface for po-Si sample. The dark region at the bottom of the photograph, with the well-defined lattice structure, is the silicon region. Note the presence of the silicon nanocrystallites 2–5 nm in size in the light-colored po-Si region. (b) High-resolution XTEM image of epoxy/po-Si interface showing nanocrystalline inclusions located at surface of po-Si layer. The epoxy region is located in the lower portion of the photograph.

approximate sampling depth of the XPS). The relationship, if any, between the reduced luminescent yield and changes in surface passivation was examined by integrating the total surface silyl hydride content before and after x-ray exposure by using FTIR. A 5–15% reduction in surface Si-H_x was observed; this indicates that the majority of the surface hydride passivation was intact even though the luminescence was virtually eliminated. From our data, it appears that the phase transition to a-po-Si (Figure 4-7) and the reduction in visible photoluminescence are related. The samples etched for 10 min showed no change in the valence band XPS signature, as mentioned earlier, but did exhibit a significant reduction in PL after x-ray exposure. This suggests that the same x-ray-induced process occurred on samples etched for 10 min, but at a depth greater than for those samples etched for only 1 min and too great (> 10 nm) for the XPS to detect.

Since the surface passivation remains essentially intact following the x-ray exposure, the phase transition must be responsible for the drastically reduced luminescence, suggesting the origin of the luminescence to be the nc-po-Si. This observation is in agreement with reports of nc-po-Si in the range 2–5 nm as being responsible for the visible light emission. For example, double-crystal x-ray diffraction of po-Si prepared from *p*-type Si has detected crystalline po-Si phases [14],[15]. Interestingly, these nanocrystalline phases exhibited lattice constant dilatations from 0.03% [14] to 0.6% [15], whereas other workers [16] observed lattice dilatations for chemical-vapor-deposited nc-Si of 0.5% for nanocrystallites 5 nm in diameter and up to 1% for Si nanocrystallites 2 nm in diameter. Thermodynamic analysis suggests lattice constant distortions approaching 1% are sufficient for driving a crystalline-to-amorphous phase transition [17], and this has been previously suggested as the origin of an amorphous phase in anodically etched po-Si [12]. The metastability of the nc-po-Si observed here may also explain why many luminescent samples appear amorphous upon inspection. It is, however, unclear what types or shapes of nanocrystals are metastable or what forms of activation are required to drive the phase transition. The thermodynamics of the nanocrystalline-to-amorphous phase transition have been analyzed [17], and the driving force for the phase transition stems from an increase in free energy resulting from the lattice dilatations.

These experiments have provided evidence for an amorphous-to-crystalline phase transition in po-Si, accompanied by a significant decrease in the photoluminescent yield. At the same time no significant chemical changes could be detected in the nature of the surface passivation. We feel these results support the theory of quantum confinement and can also explain much of the previous, apparently contradictory, data published in the literature. For example, previous reports [18] using μ-PL average over areas that may well contain both amorphous and crystalline phases, making it difficult to attribute a specific morphology to the luminescent region. Previous XTEM studies have identified po-Si as both crystalline [19] and amorphous [20], perhaps indicative of effects of the preparation conditions on the po-Si morphology.

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REFERENCES

1. G. N. Taylor, L. E. Stillwagon, and T. Venkatesan, *J. Electrochem. Soc.* **131**, 1658 (1984).
2. M. A. Hartney, M. Rothschild, R. R. Kunz, D. J. Ehrlich, and D. C. Shaver, *J. Vac. Sci. Technol. B* **8**, 1476 (1990).
3. S. C. Palmateer, R. R. Kunz, A. R. Forte, and M. Rothschild, *Proc. SPIE* **2438**, 455 (1991).
4. N. Benjamin, B. Chapman, and R. Boswell, *Proc. SPIE* **1392**, 95 (1990).
5. Solid State Research Report, Lincoln Laboratory, MIT, 1995:2, p. 21.
6. Low Entropy Systems, Inc., Somerville, Mass.
7. E. Yablonovitch, D. L. Allara, C. C. Chang, T. Gmitter, and T. B. Bright, *Phys. Rev. Lett.* **57**, 249 (1986).
8. P. Gupta, V. L. Colvin, and S. M. George, *Phys. Rev. B* **37**, 8234 (1988).
9. R. P. Vasquez, A. Madhukar, and A. R. Tanguay, Jr., *J. Appl. Phys.* **58**, 2337 (1985).
10. J. E. Rowe and H. Ibach, *Phys. Rev. Lett.* **32**, 421 (1974).
11. E. O. Kane, *Phys. Rev.* **146**, 558 (1966).
12. R. P. Vasquez, R. W. Fathauer, T. George, A. Ksendov, and T. L. Lin, *Appl. Phys. Lett.* **60**, 1004 (1992).
13. L. T. Canham, *Appl. Phys. Lett.* **57**, 1046 (1990).
14. I. M. Young, M. I. J. Beale, and J. D. Benjamin, *Appl. Phys. Lett.* **46**, 1133 (1985).
15. K. Barla, R. Herino, G. Bomchil, J. C. Pfister, and A. Freund, *J. Cryst. Growth* **68**, 727 (1984).
16. S. Veprek, Z. Iqbal, H. R. Oswald, F. A. Sarott, J. J. Wagner, and A. P. Webb, *Solid State Commun.* **39**, 509 (1981).
17. S. Veprek, Z. Iqbal, and F. A. Sarott, *Philos. Mag. B* **45**, 137 (1982).
18. N. Noguchi, I. Suemune, M. Yamanishi, G. C. Hua, and N. Otsuka, *Jpn. J. Appl. Phys.* **31**, L490 (1992).
19. A. G. Cullis and L. T. Canham, *Nature* **353**, 335 (1991).
20. T. George, M. S. Anderson, W. T. Pike, T. L. Lin, R. W. Fathauer, K. H. Jung, and D. L. Kwong, *Appl. Phys. Lett.* **60**, 2359 (1992).

5. HIGH SPEED ELECTRONICS

5.1 FIELD-EMITTER ARRAYS FOR MICROWAVE-TUBE CATHODES

Field-emitter arrays (FEAs) are being developed for use as cathodes in microwave tubes. Microwave tubes with FEA cathodes provide higher-frequency performance and faster turn-on than tubes with conventional gated thermionic cathodes and deliver higher-power output than solid state devices.

The FEA development is part of a larger effort, led by Varian, to demonstrate a 10-GHz klystrode [1]. The klystrode specifications require an emitter array that delivers 160 mA of current and is disposed within the ~ 0.030-in. diameter of the klystrode electron-beam tunnel. For this purpose, a previously reported FEA fabrication process [2] based on laser-interferometric lithography is being optimized to produce arrays of gated Mo cones having 0.32-μm tip-to-tip and 0.08-μm gate-to-tip spacings. The small dimensions and high density of the tips reduce the required input drive voltages, increase FEA transconductance, and shrink array size, providing better input impedance characteristics, electron-beam quality, and higher klystrode gain. Arrays comprising four 30-μm-long by 240-μm-wide annular array segments disposed around a 0.024-in.-diam circle have been designed to meet the klystrode requirement.

A number of FEA processing improvements have been carried out. Figure 5-1 illustrates two areas in which the improvements were made. First, the thickness of the gate metal was increased from 400 to 700 Å, as shown in Figure 5-1(b). This reduces the gate resistance and eliminates stress-induced wrinkles

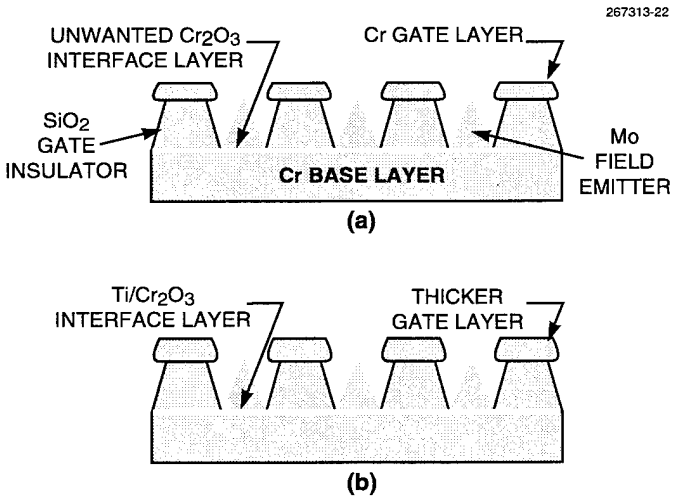

Figure 5-1. Important recent improvements to field-emitter array (FEA) processing: (a) previous tip construction showing unwanted Cr_2O_3 layer formed during SiO_2 deposition and (b) improved tip construction in which gate-layer thickness is increased and adverse effects of Cr_2O_3 insulating interface layer are eliminated.

in the gate film. Second, an additional Ti layer was inserted at the base of the cones, as shown in Figure 5-1(b), which breaks down and/or penetrates the Cr_2O_3 layer, thereby preventing it from acting as a barrier to electron flow. Test-structure measurements indicated that an insulating Cr_2O_3 layer was formed at the base of the emitting cones as a result of the SiO_2 gate-insulator deposition, as shown in Figure 5-1(a). Figure 5-2 shows a scanning electron micrograph of a recent FEA.

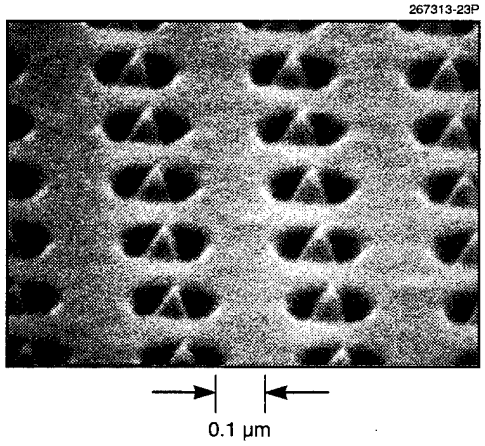

Figure 5-2. FEA made using improved processing. Note the thicker, smoother gate.

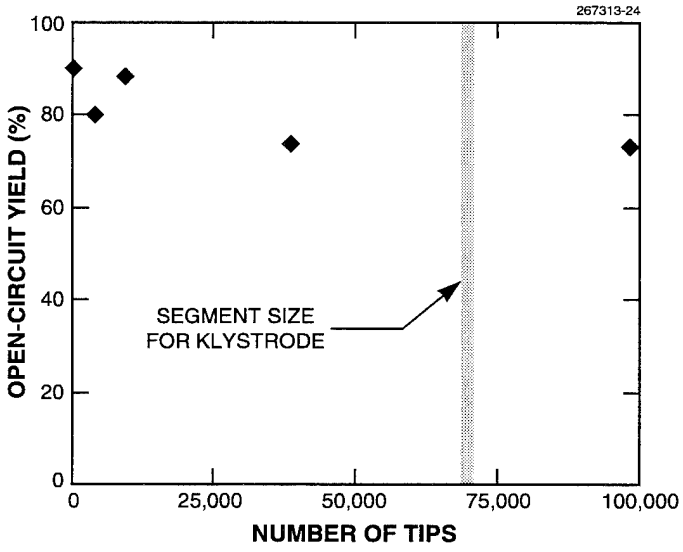

Figure 5-3. Yield estimated from gate-base open-circuit devices on wafer 8LC1-2. The array size required for the klystrode application is noted.

FEA wafers fabricated with these improvements have displayed high yield. Figure 5-3 plots the percentage of FEA devices with open-circuit gate-base characteristics as a function of the number of tips in the device. For an array segment of the size needed for the klystrode application, a yield of ~ 74% is predicted. Extrapolation of the highest emission current densities seen so far in small single-segment devices suggests that emission currents up to 48 mA should be achievable in the full annular arrays for the present emitter design and emitter-tip surface conditioning. Present efforts are focused on developing improved surface-conditioning procedures that will ensure that 160 mA can be achieved in the klystrode environment.

In the klystrode application, the input drive voltage must be coupled to the emitting tips with acceptable dissipative and mismatch losses. Simulations [3],[4] indicate that phase-delay and attenuation effects in FEA segments will be negligible for array lengths < 50 μm, and that an RF gate-voltage swing of ~ 10 V will produce useful klystrode output power and gain.

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REFERENCES

1. D. H. Priest and M. B. Shrader, *IEEE Trans. Electron Devices* **38**, 2205 (1991).
2. C. O. Bozler, C. T. Harris, S. Rabe, D. D. Rathman, M. A. Hollis, and H. I. Smith, *J. Vac. Sci. Technol. B* **12**, 629 (1994).
3. J. P. Calame, H. F. Gray, and J. L. Shaw, *J. Appl. Phys.* **73**, 1485 (1993).
4. C. O. Bozler, D. D. Rathman, C. T. Harris, G. A. Lincoln, R. H. Mathews, S. Rabe, R. A. Murphy, and M. A. Hollis, *International Vacuum Microelectronics Conference Technical Digest* (IEEE, Piscataway, N.J., 1995), p. 118.

6. MICROELECTRONICS

6.1 MEASUREMENTS OF QUANTUM EFFICIENCY AND OPTICAL RESPONSE UNIFORMITY IN A WAFER-SCALE BACK-ILLUMINATED CCD IMAGER

In recent reports [1],[2] we have described a large, frame-transfer charge-coupled device (CCD) imager developed for the GEODSS (Ground-based Electro-Optical Deep Space Surveillance) system to acquire and track space objects. The goal of this development is a back-illuminated version of the device, which can offer a 2–3 times increase in sensitivity compared to a conventional front-illuminated CCD. We have described previously some of our work in the area of back illumination [3],[4], with particular emphasis on the treatment of the back (etched) surface. We present here an updated description of one of the processes we have developed [3], as well as quantum efficiency (QE) and optical uniformity data from the imagers.

The fabrication of a back-illuminated CCD imager begins with a completed front-illuminated CCD. At this stage a device is tested in a wafer-probe station to assure good performance, and then the front surface is capped with a thick layer of SiO_2 to protect the device during subsequent process steps. The wafer is then chemically thinned from the back surface to the desired thickness, usually about 20 μm. The etching process does not depend on selectivity to achieve the desired final thickness, as in some processes that require the use of p/p^+ epitaxial layers and an etchant that attacks the p^+ at a much higher rate than the lightly doped epilayers. We are able to achieve final device thicknesses uniform to $\pm$ 1 μm with nonselective etching and therefore can apply this process to homogeneously doped silicon of any resistivity.

After the wafer is thinned, it is mounted circuit-side down with epoxy onto another silicon wafer for mechanical support. The next step is a treatment of the etched surface to minimize recombination loss of photoelectrons to surface states. Boron is implanted into this side to form a p^+ layer that produces an electrostatic barrier to electrons. To activate the implant we use a KrF excimer laser operating at 248 nm. The light generated by this laser is spread across a square area on the wafer with sides $L \approx 6$ mm. The flux is quite uniform in the center of the beam but decreases towards the edges. In order to make the QE of the annealed device more uniform, we have used different schemes for overlapping the laser pulses. One of these patterns is shown in Figure 6-1, where the laser is stepped in increments of $L/2$ in both x and y. This pattern anneals the entire wafer four times, but the optical sensitivity at 600 nm at the boundaries of these pulses can vary by as much as 50% with an rms variation of ~ 15%. A more recent and improved pattern is shown in Figure 6-2. It consists of four sets of step-and-repeat anneals, each offset in x and y by $L/4$.

The thin silicon of the CCD as well as oxide layers at the perimeter of the device are now etched away to expose the aluminum bonding pads. One important role of the capping SiO_2 layer is to provide mechanical support under the aluminum pads during wire bonding, since the epoxy is somewhat soft. The final steps include an evaporated aluminum light shield covering all but the imaging portion of the device and the deposition of an antireflection (AR) coating.

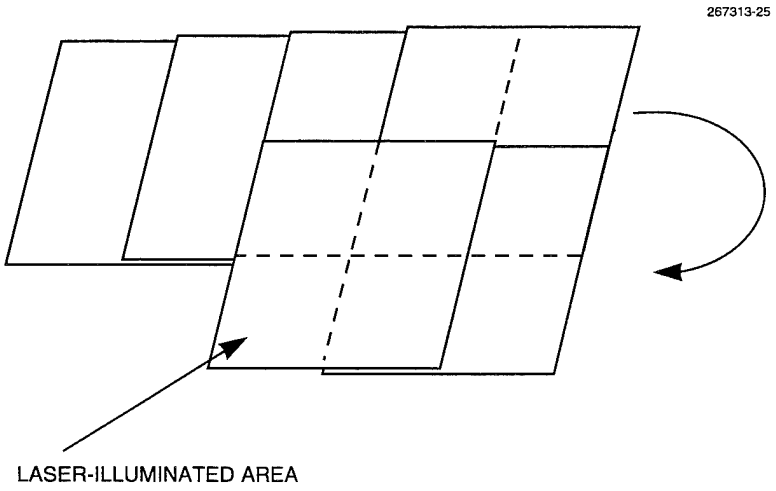

Figure 6-1. Step-and-repeat pattern of one of the laser anneal processes. Each square represents one flash of the laser and measures ~ 6 × 6 mm.

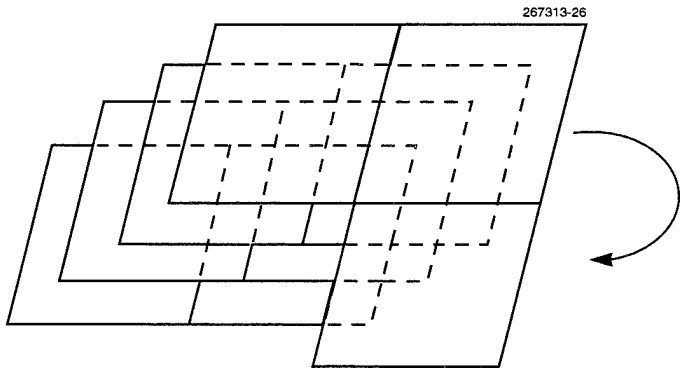

Figure 6-2. Another laser anneal stepping pattern with improved anneal uniformity.

We have measured the QE using a method described previously [5]. The data in Figure 6-3 taken at –50°C are typical of results from several devices, each of which had an AR coating of approximately 75 nm of SiO. As seen in the Figure, the QE has a broad maximum around 600 nm corresponding to $\lambda/4$ of the coating. Toward the near-infrared the falling QE is due not only to the mismatch of the AR coating but also to the decreasing absorption of the radiation in the 20 μm of silicon. The reduced QE in the ultraviolet (UV) is due to the AR coating mismatch as well as the onset of significant absorption in the SiO below 450 nm. Another factor limiting the UV response for this process is the very shallow absorption depth of the photons below 400 nm; the resulting recombination losses at the back surface are therefore quite high in this wavelength regime. However, this low sensitivity is not detrimental for viewing sun-illuminated space objects from the ground, since the atmosphere absorbs much of the UV. For comparison, we have also plotted the QE of the S-20 photocathode used in the Ebsicon tubes now deployed at the GEODSS sites. A useful QE metric for space surveillance is the average QE from 300 to 1000 nm weighted by the solar photon flux at air mass zero. The value of this average for the CCD is ~ 65%, while for the S-20 it is only 6%.

We have measured the optical response uniformity by illuminating each of the four quadrants (a quadrant comprises 980 × 1280 pixels) and digitally recording the image data. Several frames were averaged to reduce photon noise to less than the spatial variation in optical response. We passed light

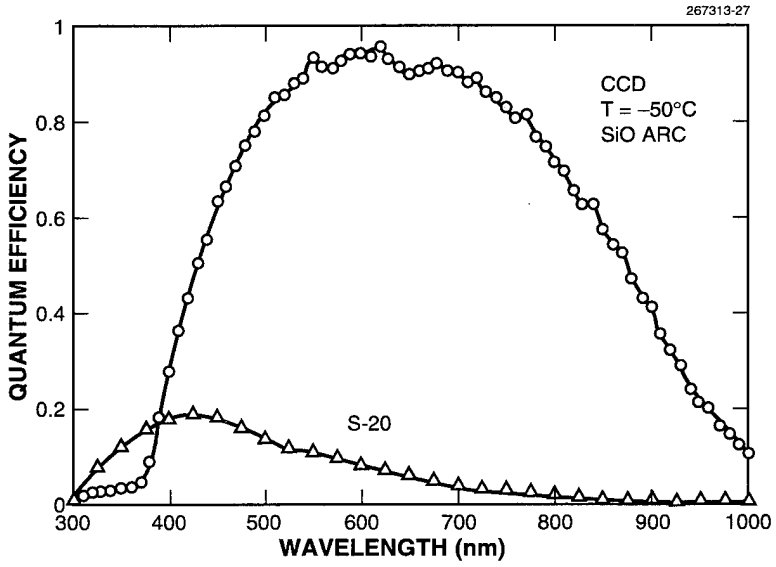

Figure 6-3. Measured quantum efficiency (QE) vs wavelength for a back-illuminated charge-coupled device imager. The QE of the S-20 photocathode used in the Ebsicon tubes now deployed at the GEODSS sites is plotted for comparison.

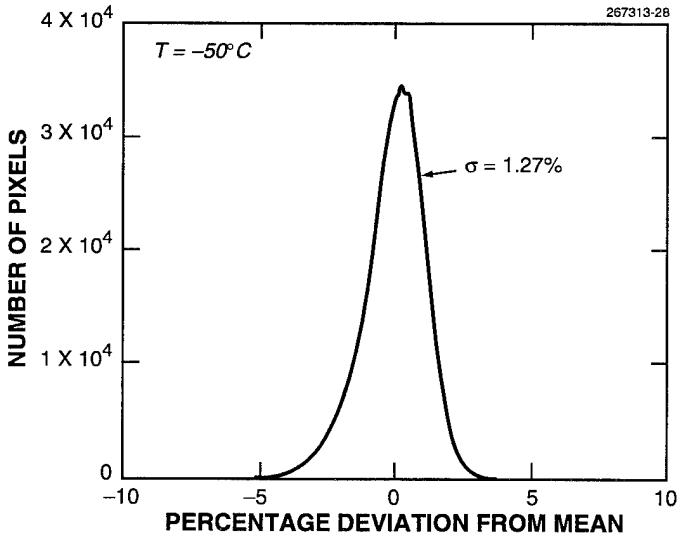

Figure 6-4. Histogram of pixel amplitudes with the device uniformly illuminated with a simulated solar spectrum. The data here were taken on a quadrant (980 × 1280 pixels) of the device.

from a tungsten-halogen lamp through a water filter to simulate a solar spectrum, while uniform illumination for the CCD was obtained by placing a thin sheet of teflon in the beam and locating the CCD several centimeters beyond the teflon. Figure 6-4 shows a histogram of the relative pixel amplitudes with the device illuminated. The rms variation indicated is ~ 1.2%, most of which was the result of slight variations in the laser anneal from the stepping pattern.

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REFERENCES

1. Solid State Research Report, Lincoln Laboratory, MIT, 1993:4, p. 39.
2. Solid State Research Report, Lincoln Laboratory, MIT, 1995:2, p. 34.
3. Solid State Research Report, Lincoln Laboratory, MIT, 1989:4, p. 61.
4. Solid State Research Report, Lincoln Laboratory, MIT, 1993:1, p. 53.
5. Solid State Research Report, Lincoln Laboratory, MIT, 1993:2, p. 27.

7. ANALOG DEVICE TECHNOLOGY

7.1 DEMONSTRATION OF A 40-ns $YBa_2CU_3O_{7-\partial}$ CHIRP FILTER ON 125-μm BONDED-WAFER $LaAlO_3$ SUBSTRATES

Compressive receivers, which implement an analog chirp transform using chirp filters, have a distinct advantage over conventional electronic warfare (EW) receivers by detecting many simultaneous signals over a wide analysis bandwidth with 100% time coverage [1]. High-temperature superconductive (HTS) chirp filters were recently used to double the instantaneous bandwidth coverage of a modern EW compressive receiver originally designed around surface-acoustic-wave (SAW) chirp filters [2]. Notably, SAW chirp filters are limited to < 1-GHz bandwidth. However, an important technical challenge for HTS chirp filters has been to increase the length of the tapped delay lines constituting the filter. The filters used in the EW receiver demonstration had only 24 ns of dispersive delay. Longer delay produces more signal processing gain in the filter and, more important, results in improved frequency resolution in the compressive receiver.

A significant milestone has now been achieved with the demonstration of a 40-ns $YBa_2Cu_3O_{7-\partial}$ (YBCO) chirp filter. This 40-ns, 2-GHz-bandwidth YBCO chirp filter has a time-bandwidth product of 80 and produces a raw frequency resolution of 40 MHz. This filter finally demonstrates sufficient signal processing gain and frequency resolution to justify development of the wider-bandwidth HTS-based compressive receiver [1]. Furthermore, a multigigahertz-bandwidth compressive receiver can now be considered using these 40-ns HTS chirp filters along with state-of-the-art high-speed semiconductor components, producing a much superior EW receiver [3]. The HTS-based compressive receiver would require lower power per gigahertz of coverage than other EW receivers and would have very impressive performance characteristics in a compact, lightweight package.

The 40-ns HTS chirp filters are based on a stripline configuration that uses two symmetrically placed ground planes on opposite sides of a pair of wafers. As a result the packing density of the delay lines and therefore the total chirp filter length are directly proportional to the thickness of the two wafers. As the wafer thickness is reduced, a support wafer is required to prevent the thin wafer from breaking. Figure 7-1 diagrams the technique used to bond and thin a 2-in.-diam $LaAlO_3$ wafer and shows a photograph of a 40-ns YBCO chirp filter fabricated using the technique. The wafer-bonding process begins with a 20-mil-thick $LaAlO_3$ upper wafer with a sputtered layer of Ti/Au (300 Å of Ti followed by 2 μm of Au) on the bottom surface, a 20-mil-thick $LaAlO_3$ base wafer with a sputtered layer of Ti/Au on the top surface, and a 10-μm-thick gold foil. The two wafers and the gold foil must be kept very clean throughout the entire process. The wafers are forced together against the gold foil in a hot press inside an oxygen atmosphere.

The top wafer is lapped to a thickness of 190 μm and then polished using chemical mechanical polishing compound to a final thickness of 125 μm. The polished surface must be compatible with epitaxial growth of YBCO. After polishing, the bonded-wafer pair is placed in a standard gas pocket heater, and growth of YBCO is performed with a cylindrical magnetron on the top surface of the thin wafer [4]. Standard YBCO patterning techniques can be used following the YBCO growth [5]. The edges of the gold foil are used to make contact to the ground plane on the bottom surface of the thin wafer. A second bonded-wafer pair is required for the upper ground plane of the stripline configuration.

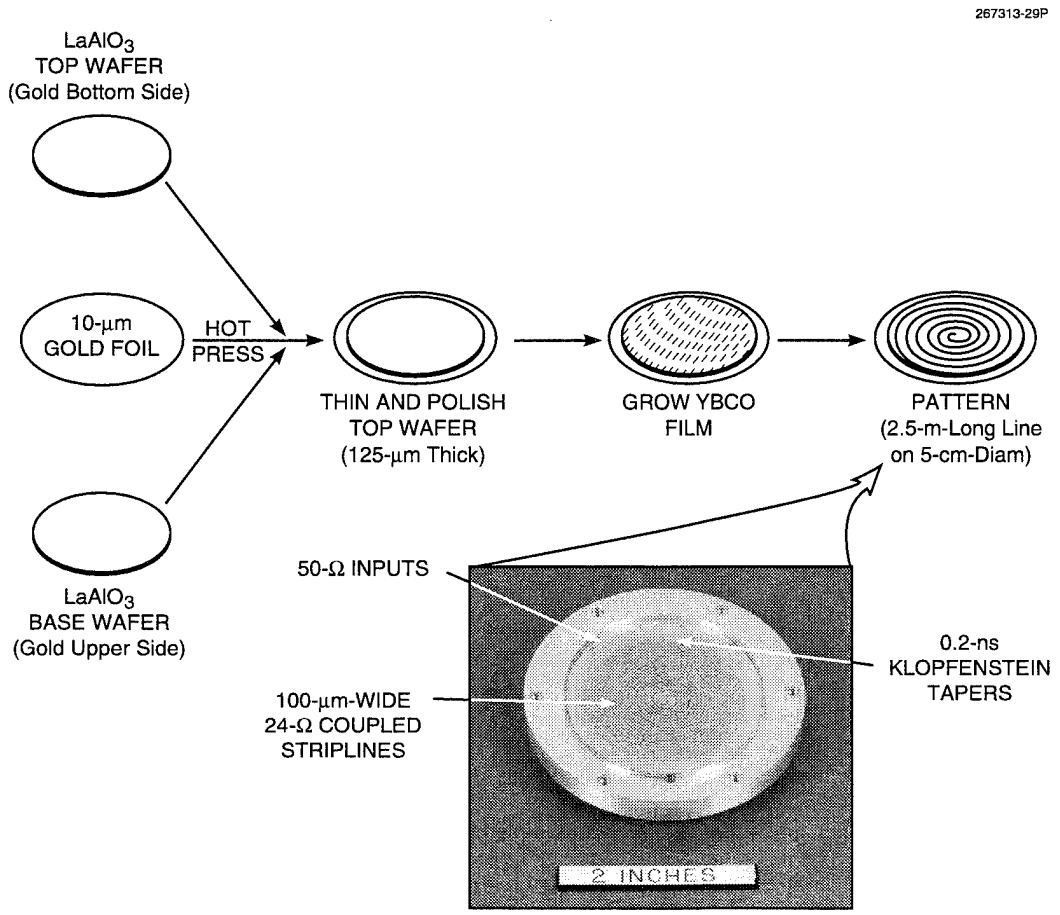

Figure 7-1. Illustration of wafer bonding and thinning technique used to fabricate 40-ns $YBa_2Cu_3O_{7-\partial}$ (YBCO) chirp filters on 125-μm-thick, 2-in.-diam $LaAlO_3$ substrates. The chirp filters are constructed using tapped delay lines in a stripline structure. A photograph of the 40-ns filter is shown as an inset.

The wafer bonding and thinning technique is validated by the performance of the 40-ns YBCO chirp filter, illustrated in Figures 7-2 and 7-3. The time-domain response of the chirp filter is shown in Figure 7-2. The time-domain reflectometry response shown is taken on one of the two transmission lines that make up the chirp filter. This is essentially a low-frequency measurement, below the cut-off frequency of the Klopfenstein impedance tapers. From left to right the response indicates a 50-Ω input connector, an inductive discontinuity from the connector to stripline transition, the taper from a 50-Ω narrow linewidth to a 24-Ω wide linewidth, a constant 24-Ω linewidth, a second taper from 24- to 50-Ω linewidth, another inductive discontinuity, and back to a 50-Ω output connector. The downchirp response to a step function is also shown. The response of each of the 160 backward-wave couplers appears, and the Hamming weighting of the couplers is evident.

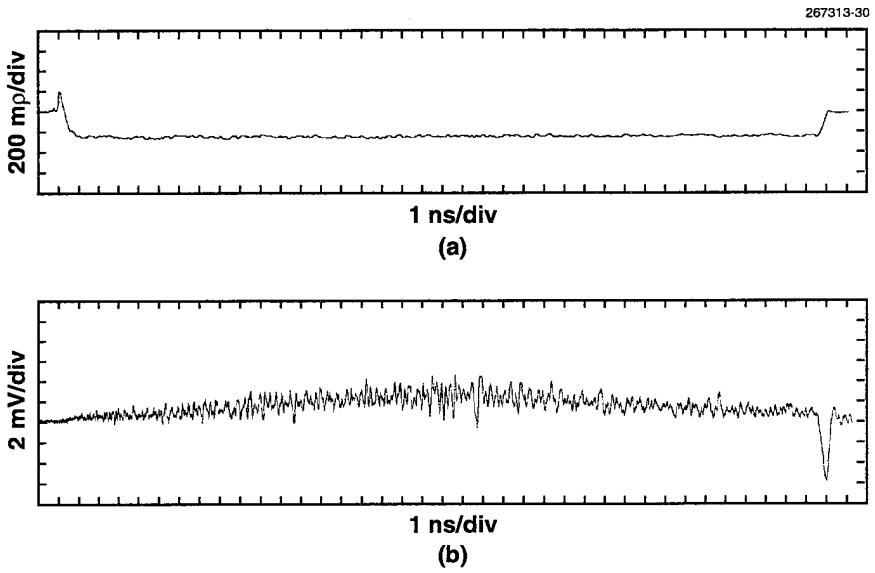

Figure 7-2. Time-domain response of 40-ns YBCO chirp filter: (a) Time-domain reflectometry measured at 77 K for one of the two YBCO striplines that constitute the 40-ns filter and (b) low-frequency time-domain response to a step function measured at 77 K using the downchirp ports of the filter.

The 40-ns YBCO chirp filter has been used to produce compressed pulses using the test setup shown in Figure 7-3(a). An upchirp waveform from the chirp generator is compressed into a pulse by the 40-ns chirp filter, acting as a downchirp filter in this configuration. The chirp generator consists of a voltage ramp generator (pulse generator, integrator, output buffer, and offset circuitry) driving a voltage-controlled oscillator to produce an 80-ns-long, 4-GHz-wide chirp waveform. The sinusoidal input signal (9–11 GHz) allows the 4-GHz-wide chirp waveform to be offset in frequency over a 2-GHz range and still produce a complete compressed pulse in the 2-GHz-bandwidth chirp filter. This input configuration, in fact, forms the basis of a compressive receiver analog front end. The compressed pulse output of the test setup is shown in Figure 7-3(b). This compressed pulse envelope has an error sidelobe level of −13 dB. A similarly configured chirp generator was previously shown to be sufficiently linear to produce −18-dB error sidelobes [6]. This indicates that the present 40-ns chirp filter is primarily responsible for the error sidelobe level. Future designs will improve this error sidelobe performance by eliminating feedthrough and spurious reflections at the input and output of the filter.

An important point is that the wafer bonding and thinning technique used here to produce 125-μm-thick, 2-in.-diam $LaAlO_3$ chirp-filter substrates can be scaled to larger areas. A 3-in.-diam, 125-μm-thick substrate would support 90 ns of dispersive delay (time-bandwidth products of 180), giving an 18-MHz frequency resolution in a compressive receiver. A 4-in.-diam, 125-μm-thick substrate would support 160 ns of dispersive delay (time-bandwidth products of 320), giving a 10-MHz frequency resolution. Such delay times would also be very useful in standard analog delay lines.

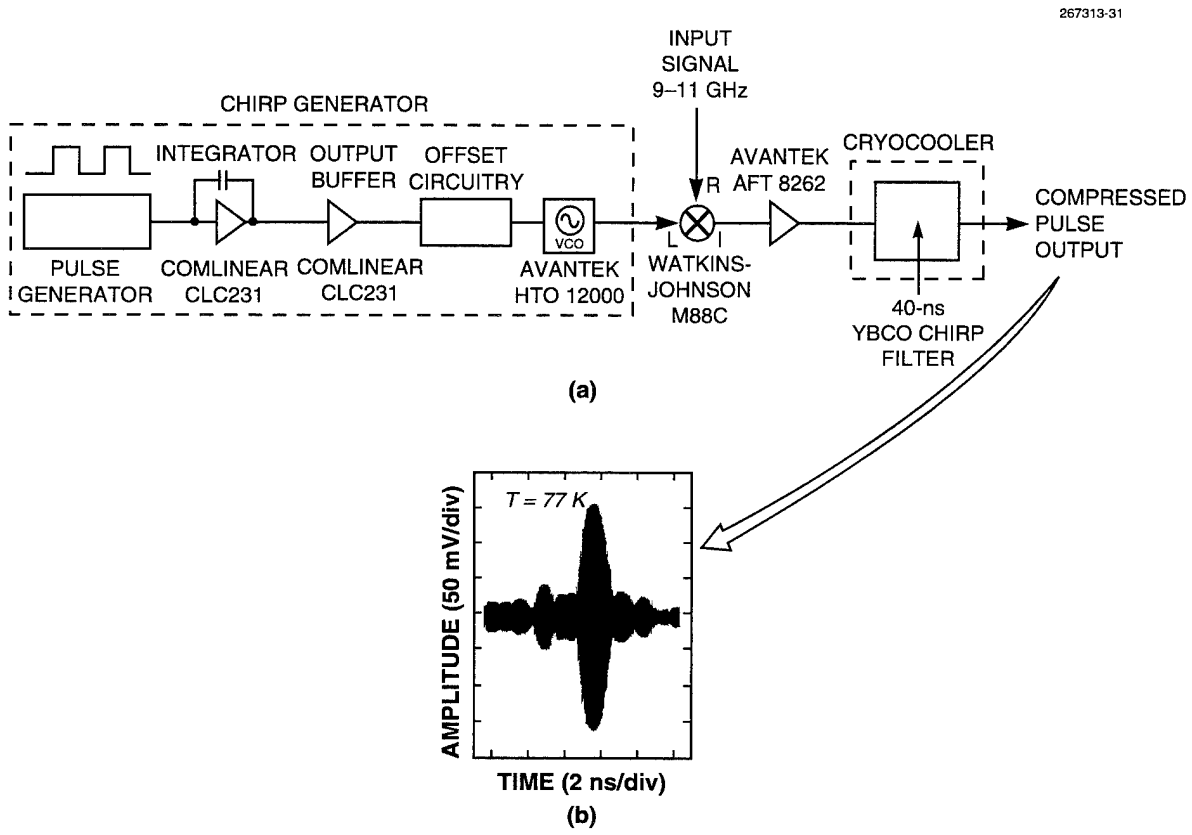

Figure 7-3. (a) Schematic diagram of compressed pulse test setup. The chirp generator is used to generate an upchirp waveform, which is then compressed into a pulse using the downchirp ports of the 40-ns YBCO chirp filter. (b) Compressed pulse envelope measured at 77 K for the test setup combination of chirp generator and 40-ns YBCO chirp filter.

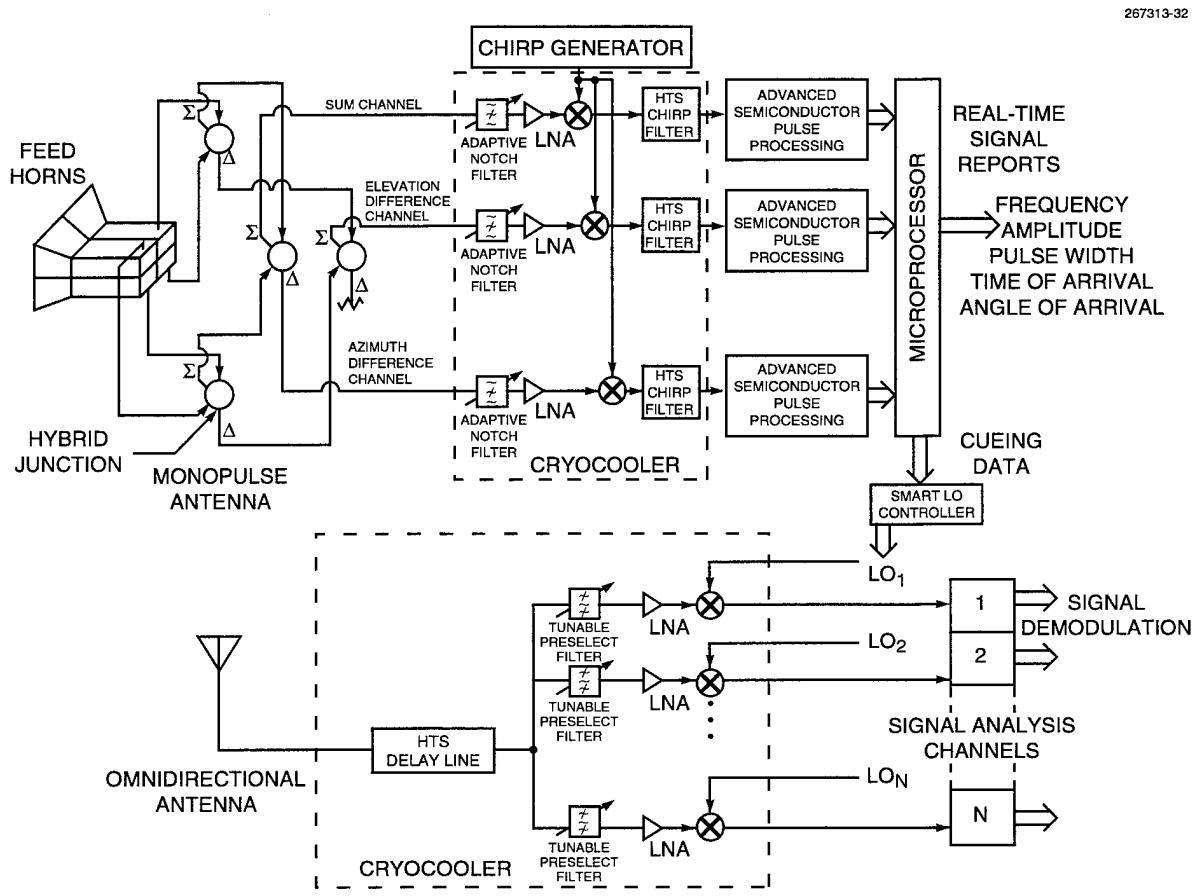

Figure 7-4. Concept for compressive cryoreceiver, including cued narrowband cryoreceivers for signal demodulation. The compressive cryoreceiver core will produce real-time signal reports of frequency, amplitude, pulse width, time of arrival, and angle of arrival. These reports will then be used to cue the narrowband cryoreceivers.

Figure 7-4 illustrates the concept for an HTS-based compressive cryoreceiver with cued narrowband cryoreceivers. The monopulse antenna allows angle of arrival to be determined using only compressed pulse amplitudes. The alternative is an interferometric antenna coupled to a measurement of the compressed pulse phase. This alternative scheme requires significantly higher speed semiconductor components and would not enhance receiver performance. The enabling devices for this receiver are HTS chirp filters with dispersive delays of 40 ns or more, and HTS standard analog delay lines of 200 ns or more. The demonstration of the 40-ns chirp filter described here has proven that both of these devices can be fabricated. Future efforts will focus on improving the accuracy of the chirp filters and scaling the wafer

bonding and thinning technique to larger-area substrates. The compressive cryoreceiver takes advantage of many aspects of cryocooled microwave components [5]. The cryocooled low-noise amplifier and mixer, the HTS adaptive notch filters, and the HTS tunable preselect filters significantly enhance the performance of the compressive cryoreceiver, but do not necessarily represent enabling devices for it.

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REFERENCES

1. K. D. Breuer, J. S. Levy, and H. C. Paczkowski, *Microwave J.* **32** (10), 81 (1989).
2. Solid State Research Report, Lincoln Laboratory, MIT, 1995:1, p. 22.
3. W. G. Lyons, D. R. Arsenault, T. C. L. G. Sollner, and R. W. Ralston, presented at IEEE MTT-S Symposium Workshop, Orlando, Fla., 15 May 1995.
4. Solid State Research Report, Lincoln Laboratory, MIT, 1993:2, p. 31.
5. N. Newman and W. G. Lyons, *J. Superconduct.* **6**, 119 (1993).
6. W. G. Lyons, D. R. Arsenault, M. M. Seaver, R. R. Boisvert, T. C. L. G. Sollner, and R. S. Withers, *IEEE Trans. Appl. Superconduct.* **3**, 2891 (1993).

8. DIGITAL INTEGRATED CIRCUITS

8.1 ADVANCED CMOS PROCESSING FOR LOW-POWER CIRCUITS AND DEVICES

The future military will depend heavily on networked, portable systems that require extensive local computation and high-bandwidth communication with minimal power dissipation. The most extreme power requirements are for remote sensors, some types of which must be extremely compact (~ 1 cm^3) and operate untethered for periods of many months. They must perform extensive signal processing for pattern recognition, but their communication rates can be very low. At the other bandwidth extreme, the individual soldier will carry a terminal that provides ready access to extensive remote, high-resolution graphics and video and hence must receive and perhaps transmit information at a prodigious rate, using spread-spectrum techniques for security and robustness. Such a terminal must be small and lightweight, ideally with voice input capability, and must operate for hours between recharges.

These two device classes represent extremes that will stretch the capabilities of microelectronic design and fabrication, so we have chosen them as the application focus for our research in advanced CMOS fabrication. Both require extensive digital computation along with the fundamentally analog functions of sensing and transmitting signals. The cost of both classes of device must be low, since they will be widely distributed. To maximize performance and minimize size, power, and cost the devices must be highly integrated and suitable for mass production. Only CMOS technology can accomplish these goals, and only the most advanced CMOS can demonstrate the concepts at convincingly high bandwidth and low power. However, CMOS fabrication at sub-0.5-μm dimensions, with the flexibility to combine ultralow power digital computation with gigahertz communication, is not available at any Department of Defense (DoD) laboratory or to most DoD contractors.

A fabrication process is being developed in the Class 10 Microelectronics Laboratory at Lincoln Laboratory to build such fast, low-power (FLP) circuits. Development is nearly complete on a 0.5-μm process in which the most critical dimension, the gate length, can be as small as 0.25 μm. An early example of the capability being developed is the rf amplifier designed in a program funded by the Advanced Research Projects Agency (ARPA) at the University of California at Berkeley, which was included on the first reticle set of the FLP program. The 1-μm version of this circuit operated successfully with a 3-dB bandwidth of 800 MHz, as illustrated in Figure 8-1.

In later fabrication runs the process was modified to produce high analog gain at deep submicrometer dimensions. Functional *n*- and *p*-channel transistors with drawn channel lengths of 0.4 μm and thresholds of 0.4 V have been built using i-line (365 nm) lithography. The ΔL of these devices is 0.1 μm, so the effective channel length is 0.3 μm. Figure 8-2 is a typical *n*-channel transistor characteristic. Presently, devices are being patterned with 248-nm lithography that will enable 0.25-μm gate length.

This advanced CMOS process will be used to enable research in both device fabrication and circuit design. In the former, for example, this development effort is highly synergistic with a program in

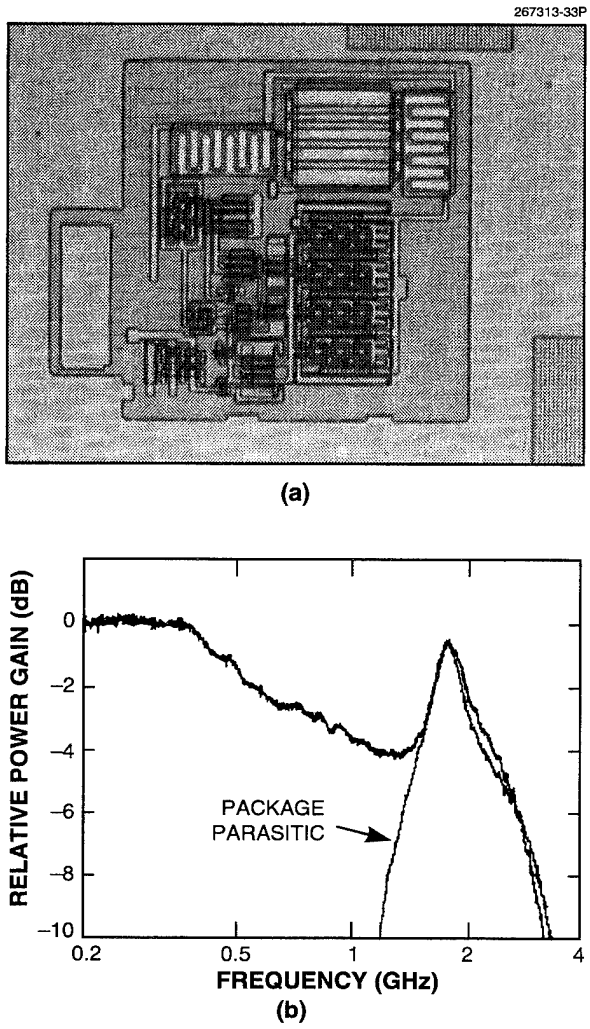

Figure 8-1. (a) Layout and (b) frequency response of CMOS amplifier designed at the University of California at Berkeley and fabricated with 1-μm minimum dimensions in Lincoln Laboratory's first fabrication run of the FLP (fast, low-power) project. The power gain rolls off by 3 dB at 800 MHz.

deep-submicron silicon-on-insulator fabrication funded by ARPA. In circuit design, both Lincoln Laboratory designers and our colleagues elsewhere in industry and universities are exploring ideas which require nonstandard, small-geometry fabrication. Based on results such as shown in the two Figures, a great deal of interest has been expressed by designers in acquiring access to such a process. We have recently completed the design of a second FLP reticle set combining circuit designs from Lincoln Laboratory system designers, Loral Infrared Imaging Systems, Sun Microsystems, Stanford, and MIT. This reticle set will be used to perfect the baseline CMOS process as well as to continue research on the variations desired by each of the users.

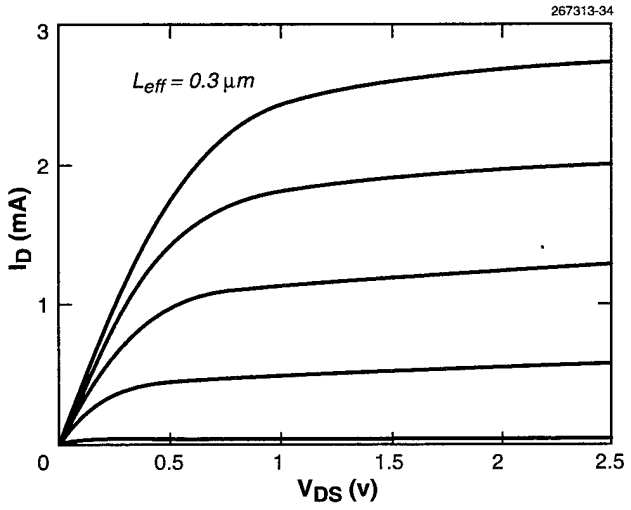

Figure 8-2. Typical transistor characteristics of n-channel MOSFET with 0.4-μm drawn gate length, 0.3-μm effective channel length, and 10-μm channel width.

The goal of the FLP program is to augment and complement the service provided to design researchers by ARPA's MOSIS foundry. MOSIS provides educational institutions and other government contractors access to conventional CMOS fabrication facilities using a relaxed set of geometric design rules. The MOSIS service has a reputation for a reliable eight-week turnaround time to deliver these fully scaled CMOS circuits. Minimum dimensions range from 2 μm (low cost, frequent runs, fast turnaround) to the recently announced 0.5 μm (considerably higher cost, infrequent runs). The user interface is simple, convenient, and completely rigid: the designer can have no influence whatsoever on the fabrication process.

In contrast, users of the Lincoln FLP process will interact directly with the fabrication engineers to evaluate how their circuit design and our process can be optimized to produce the best result. For example, process modifications to fabricate circuits with multiple transistor thresholds, high- and low-voltage devices, double-polysilicon layers, micromachined inductors, or multiple gate oxide thicknesses are possible. The modifications required for a particular application will be determined initially using PDSIM, a process and device simulation system developed at Lincoln Laboratory. PDSIM automatically sets up an array of factorially designed experiments to run on commercial simulators and associates the predicted electrical behavior with process inputs such as implant doses and oxidation times. Over time, a set of readily available process variations will be developed, with the emphasis determined by user needs.

The present process was aimed at 0.4-V thresholds for operation with a 2-V power supply. It used an i-line stepper that can reliably produce 0.5-μm geometries for most layers and 0.4 μm for the polysilicon gates. PDSIM was used extensively to develop a process that includes 8-nm gate oxides, dual-doped

polysilicon gates, oxide sidewall spacers, $TiSi_2$-clad poly and source/drain regions, and junctions activated by rapid thermal annealing. Two levels of metal are utilized, with the interlevel dielectric planarized by chemical mechanical polishing. Development emphasis now is on lower threshold voltage for < 1-V power supply, optimization of field isolation (comparing conventional local oxidation of silicon [LOCOS] with poly-buffered LOCOS), and additional metal layers.

The first fabrication run using the second FLP reticle set has just begun. In this work a 248-nm stepper, which can reliably produce 0.35-μm dimensions in production and 0.25 μm in the laboratory, will be utilized for the critical two levels of polysilicon and for contact cuts. These reticles will be used to determine and improve the fabrication yield of large circuits as well as to continue device optimization.

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